

# GSM3368ASF

## 30V N-Channel Enhancement Mode MOSFET

### Product Description

The N-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

The device is well suited for high efficiency fast switching applications.

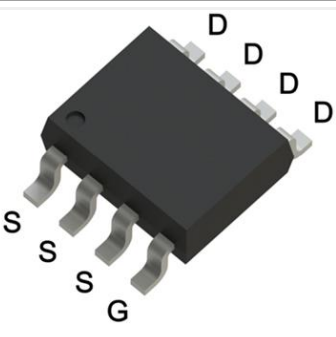
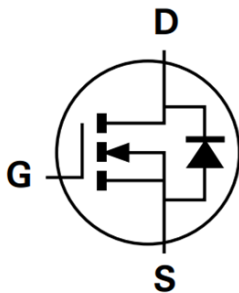
### Features

- $R_{DS(ON)} = 6m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} = 9.8m\Omega @ V_{GS} = 4.5V$
- SOP-8 Package

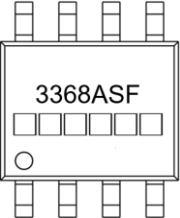
### Applications

- MB / VGA / Vcore
- POL
- SMPS

### Packages & Pin Assignments

GSM3368ASF (SOP-8)		Equivalent Circuit
		
Pin	Description	
1	Source	
2	Source	
3	Source	
4	Gate	
5	Drain	
6	Drain	
7	Drain	
8	Drain	

## Ordering and Marking Information

Ordering Information			
Part Number	Package	Part Marking	Quantity / Reel
GSM3368ASF	SOP-8	3368ASF □□□□□□	4,000 PCS
<b>GSM3368A</b> <span style="border: 1px solid black; padding: 0 2px;">1</span> <span style="border: 1px solid black; padding: 0 2px;">2</span>			
- <b>Product Code:</b> GSM3368A		- <b>Package Code:</b> <span style="border: 1px solid black; padding: 0 2px;">1</span> is <b>S</b> for SOP-8	
- <b>Green Level:</b> <span style="border: 1px solid black; padding: 0 2px;">2</span> is <b>F</b> for RoHS Compliant and Halogen Free			
Marking Information			
		- <b>Product Code:</b> 3368ASF	
		- <b>GS Code:</b> □□□□□□	

## Absolute Maximum Ratings

T<sub>A</sub>=25°C, unless otherwise specified

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current <sup>1</sup>	T <sub>A</sub> =25°C	13
		T <sub>A</sub> =70°C	10
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	65	A
P <sub>D</sub>	Total Power Dissipation <sup>3</sup>	T <sub>A</sub> =25°C	1.5
		T <sub>A</sub> =70°C	1
T <sub>J</sub>	Operating Junction Temperature Range	-55 to +150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient <sup>1</sup>	80	°C/W

Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150°C junction temperature.

## Electrical Characteristics

TA=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	-	2.5	V
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	-	4.2	6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	5.6	9.8	
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
<b>Dynamic characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	-	2295	2750	pF
C <sub>oss</sub>	Output Capacitance		-	267	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	210	-	
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	-	1.7	-	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	39	56	nC
Q <sub>gs</sub>	Gate-Source Charge		-	7.6	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	7.2	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, R <sub>g</sub> =3.3Ω, I <sub>D</sub> =10A	-	7.8	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	15	-	
t <sub>d(off)</sub>	Turn-Off Delay Time		-	37	-	
t <sub>f</sub>	Turn-Off Fall Time		-	11	-	

## Typical Performance Characteristics

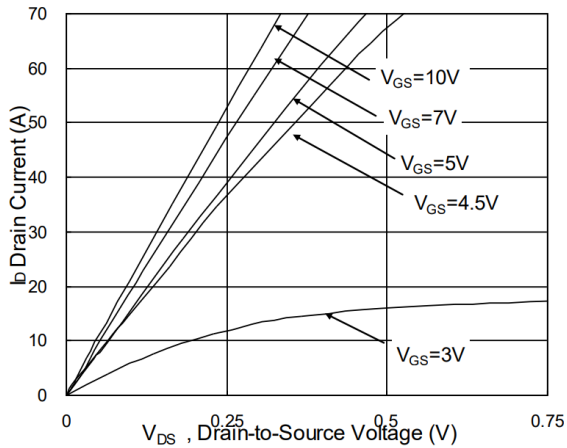


Figure 1. Typical Output Characteristics

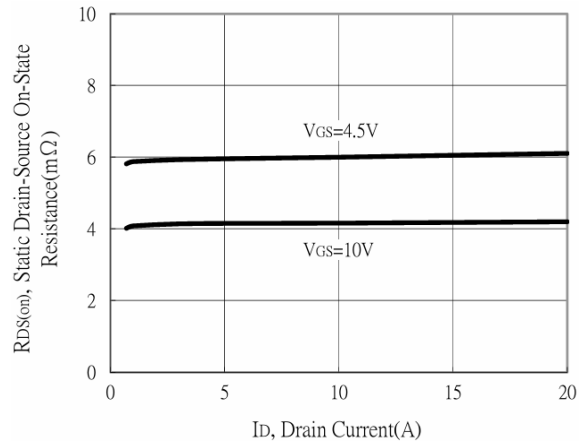


Figure 2. Drain-Source On-State resistance vs Drain Current

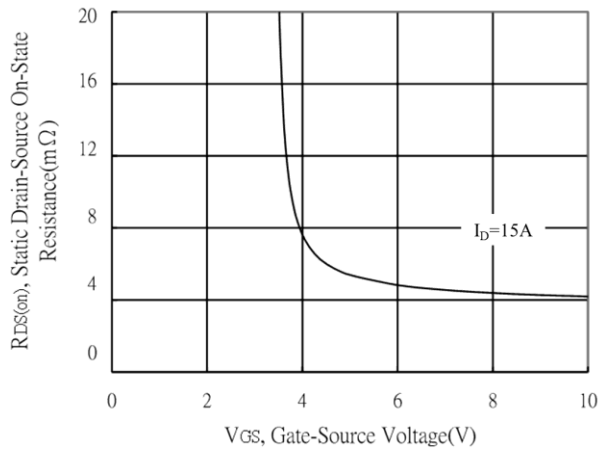


Figure 3. Drain-Source On-State Resistance vs Gate-Source Voltage

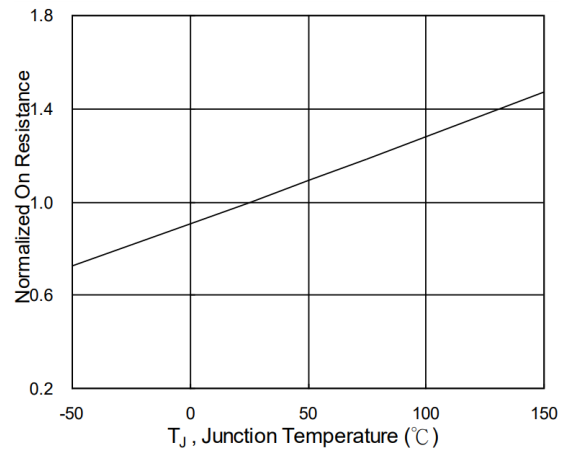


Figure 4. Drain-Source On-State Resistance vs Junction Temperature

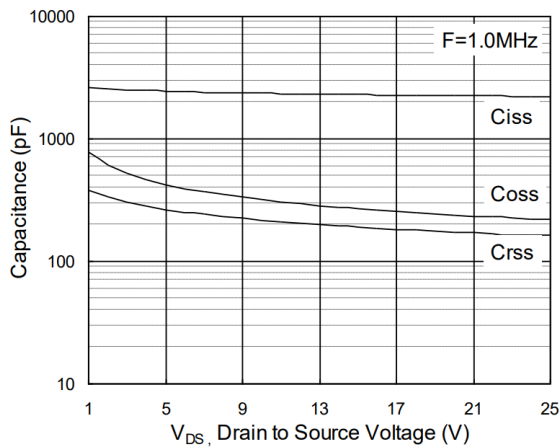


Figure 5. Capacitance vs Drain-to-Source Voltage

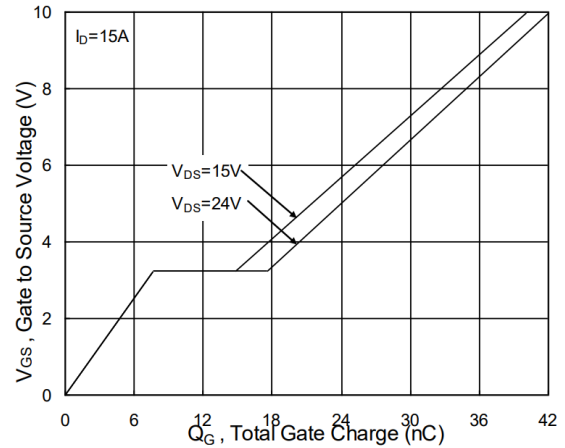


Figure 6. Gate Charge

## Typical Performance Characteristics

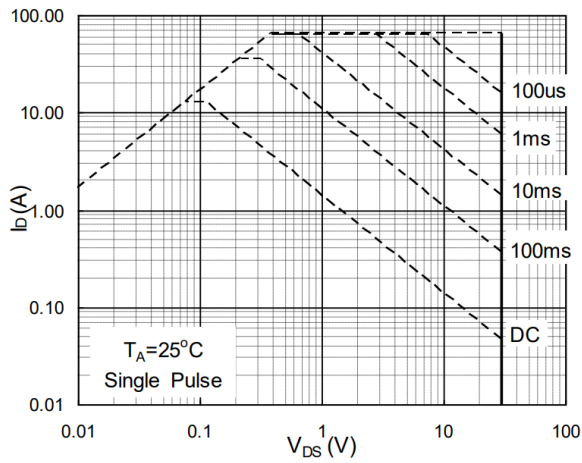


Figure 7. Maximum Safe Operating Area

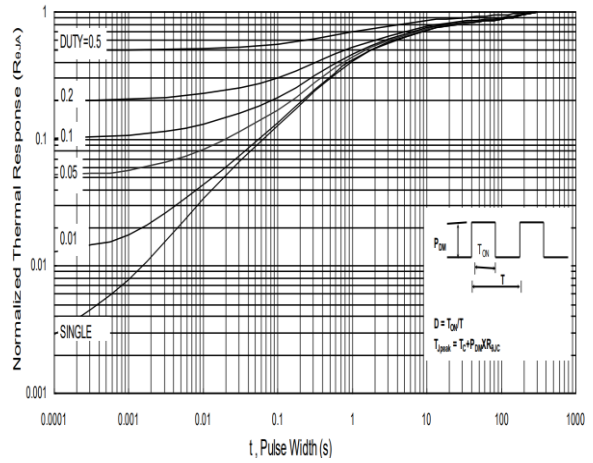
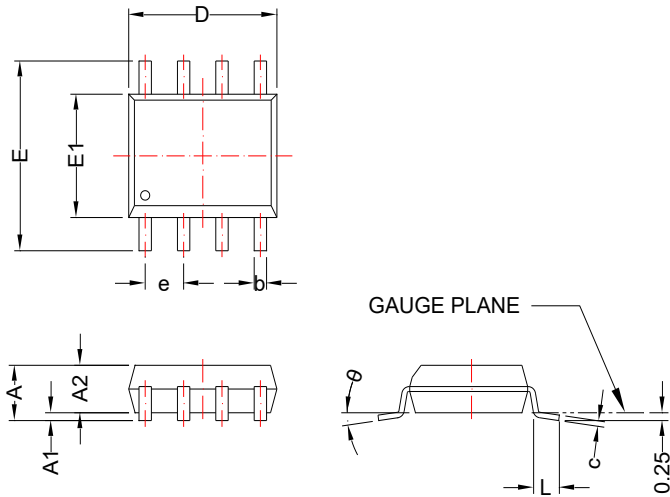


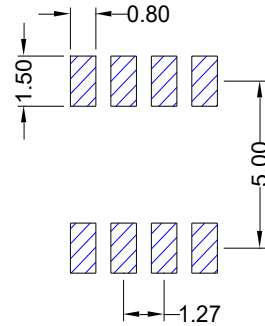
Figure 8. Normalized Transient Thermal Resistance

# SOP-8

## Package Dimension



## Recommended Land Pattern







Dimensions				
Symbol	Millimeters		Inches	
	MIN	MAX	MIN	MAX
<b>A</b>	-	1.75	-	0.069
<b>A1</b>	0.10	0.25	0.004	0.010
<b>A2</b>	1.25	-	0.049	-
<b>b</b>	0.31	0.51	0.012	0.020
<b>c</b>	0.10	0.25	0.004	0.010
<b>D</b>	4.70	5.10	0.185	0.201
<b>E</b>	5.80	6.20	0.228	0.244
<b>E1</b>	3.80	4.00	0.150	0.157
<b>e</b>	1.27 BSC		0.050 BSC	
<b>L</b>	0.4	1.27	0.016	0.050
<b>θ</b>	0°	8°	0°	8°



NOTE:  
 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.

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## CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd Neihu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587