GSM7002KAF

60V N-Channel Enhancement Mode MOSFET

Product Description

GSM7002K, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

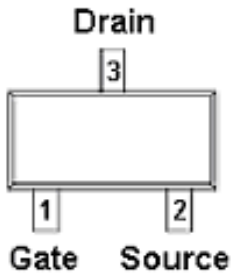
- 60V/0.5A , $R_{DS(ON)}$=3.0Ω@V_{GS}=10V
- 60V/0.2A , $R_{DS(ON)}$=4.0Ω@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-723 package design

Applications

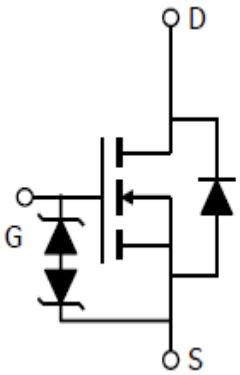
- Drivers:Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability.
  Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

Packages & Pin Assignments

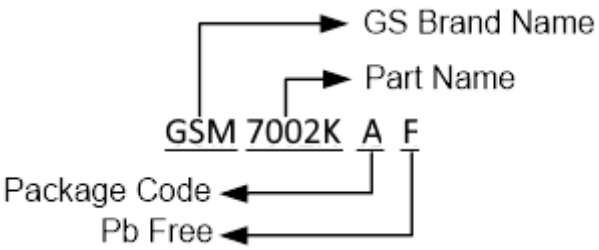
GSM7002KAF (SOT-723)



Pin	Description
1	Gate
2	Source
3	Drain



Ordering and Marking Information



Part Number	Package	Part Marking	Quantity
GSM7002KAF	SOT-723	RK	8000 PCS

Absolute Maximum Ratings

T_A=25ºC Unless otherwise noted

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage - Continuous		±20	V
I_D	Continuous Drain Current	T_A=25℃	0.15	A
		T_A=70℃	0.13	
P_D	Power Dissipation	T_A=25℃	0.16	W
		T_A=70℃	0.1	
T_J	Operating Junction Temperature		-55/150	ºC
T_{STG}	Storage Temperature Range		-55/150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		833	ºC/W

Electrical Characteristics

T_A=25ºC unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.0		2.0	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			10	uA
		V_{DS}=0V, V_{GS}=±10V			200	nA
		V_{DS}=0V, V_{GS}=±5V			100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	uA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=0.5A		1.3	3	Ω
		V_{GS}=4.5V, I_D=0.2A		1.4	4	
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=0.2A		0.97	1.5	V
Q_{rr}	Recovered Charge	V_{GS}=0V, I_S=300mA, V_R=25V dI/dt=-100A/μs		30		nC
t_{rr}	Reverse Recovery Time	V_{GS}=0V, I_S=300mA, V_R=25V, dI/dt=-100A/μs		30		ns
Dynamic						
Q_g	Total Gate Charge	V_{DD}=10V, I_D=0.25A, V_{GS}=4.5V		500		pC
Q_{gs}	Gate-Source Charge			100		
Q_{gd}	Gate-Drain Charge			150		
C_{iss}	Input Capacitance	V_{DS}= 25V, f =1MHz, V_{GS}=0V		30		pF
C_{oss}	Output Capacitance			8		
C_{rss}	Reverse Transfer Capacitance			5		
$t_{d(on)}$	Turn-On Time	V_{DD}=30V, I_D=0.2A, R_G=10Ω, V_{GEN}=4.5V, R_L=150Ω		10	20	ns
t_r				35	50	
$t_{d(off)}$	Turn-Off Time			20	30	
t_f				40	60	

Typical Performance Characteristics

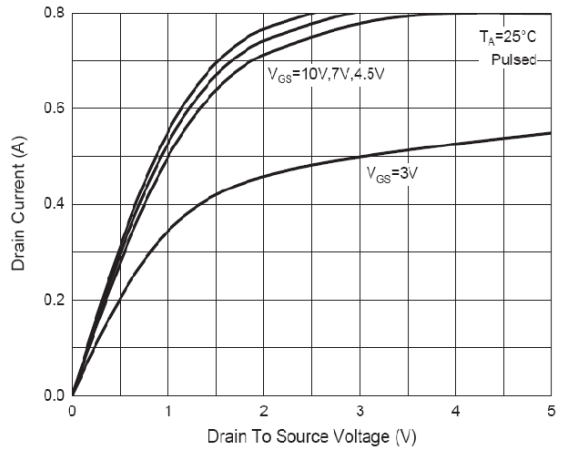


Fig. 1 Typical Output Characteristics

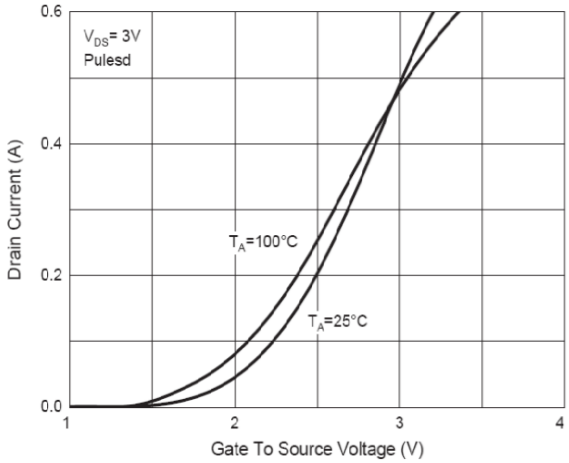


Fig. 2 Typical Transfer Characteristics

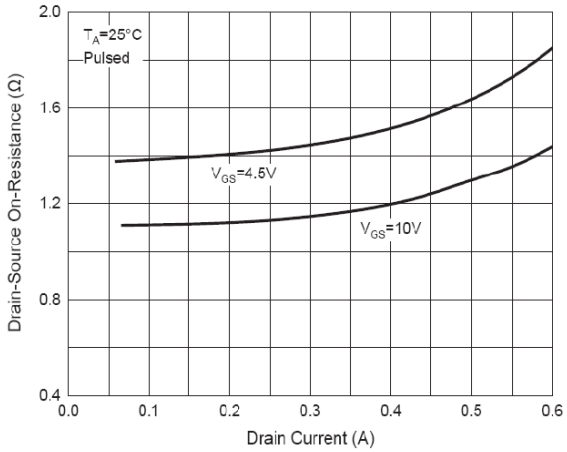


Fig.3 Typical On-Resistance vs. Drain Current and Gate Voltage

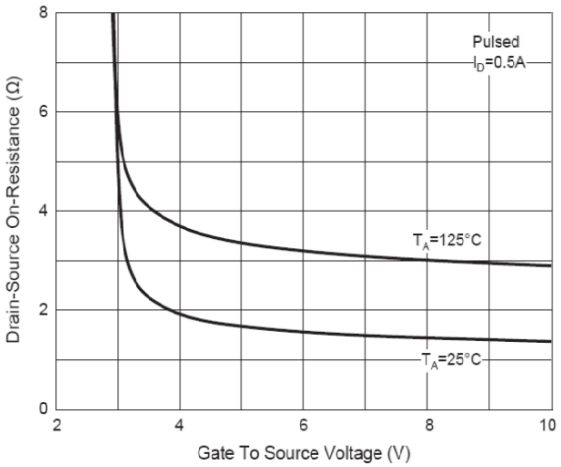


Fig.4 Typical Transfer Characteristic

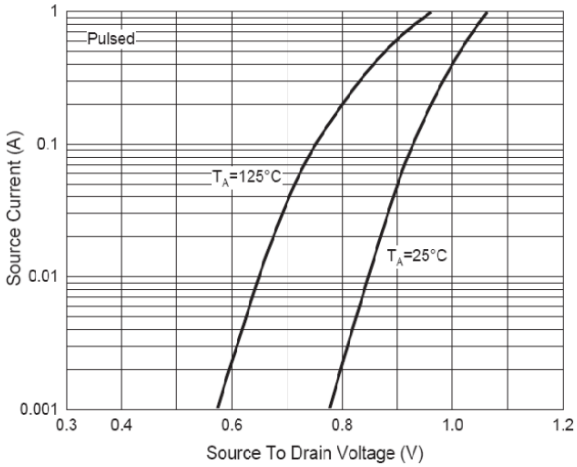


Fig.5 Diode Forward Voltage vs. Current

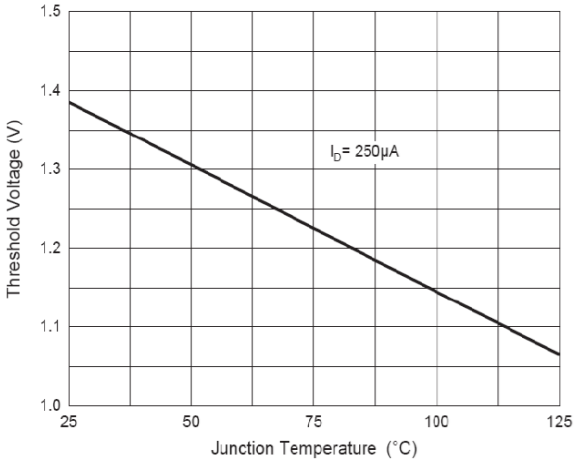
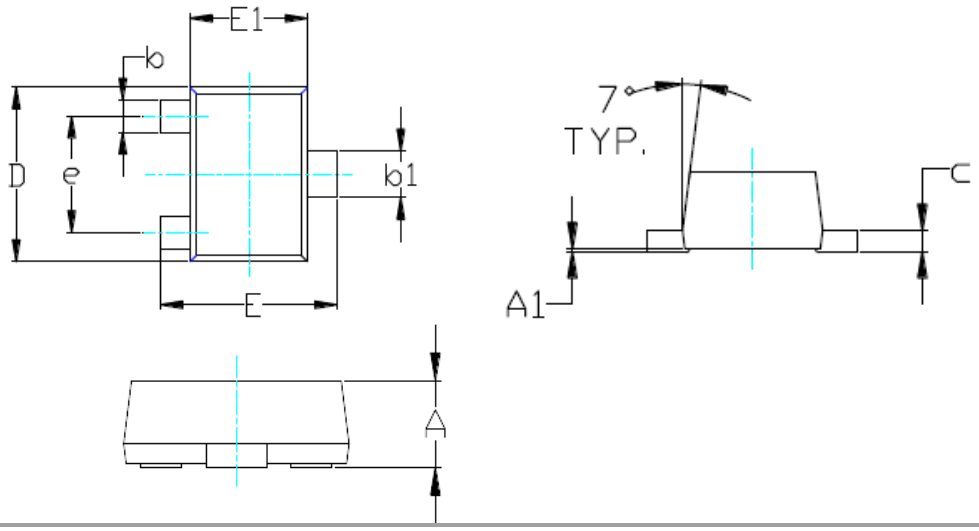


Fig.6 Gate Threshold Variation vs. T_J

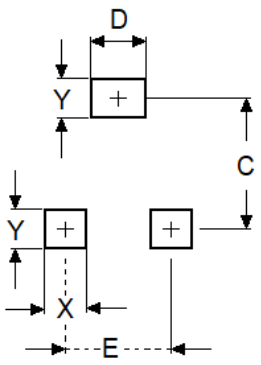
Package Dimension

SOT-723



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.430	0.500	-	0.020
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
b1	0.270	0.370	0.011	0.015
c	0.080	0.150	-	0.006
D	1.150	1.250	0.045	0.049
E	1.150	1.250	0.045	0.049
E1	0.750	0.850	0.030	0.033
e	0.800 TYP		0.031 TYP	
θ	7° REF		7° REF	

Suggested Pad Layout



DIMENSIONS	*VALUE (IN MM)*
C	1.00
D	0.42
E	0.80
X	0.32
Y	0.30

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