GSM6601

30V N & P Pair Enhancement Mode MOSFET

Product Description

GSM6601, N & P Pair enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

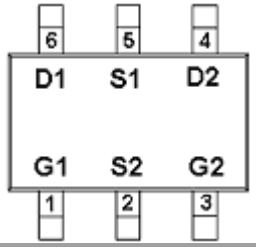
- N-Channel
  30V/3.4A, $R_{DS(ON)}$=55mΩ@V_{GS}=10V
  30V/3.0A, $R_{DS(ON)}$=65mΩ@V_{GS}=4.5V
  30V/2.0A, $R_{DS(ON)}$=85mΩ@V_{GS}=2.5V
- P-Channel
  -30V/-2.3A, $R_{DS(ON)}$=115mΩ@V_{GS}=-10V
  -30V/-2.0A, $R_{DS(ON)}$=145mΩ@V_{GS}=-4.5V
  -30V/-1.0A, $R_{DS(ON)}$=200mΩ@V_{GS}=-2.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TSOP-6 package design

Applications

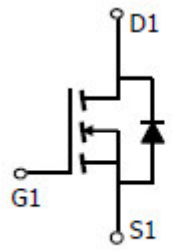
- Power Management in Notebook
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

Packages & Pin Assignments

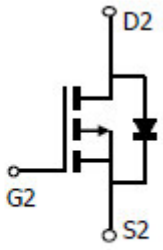
GSM6601TSF (TSOP-6)



Pin	Symbol	Description
1	G1	Gate 1
2	S2	Source 2
3	G2	Gate 2
4	D2	Drain 2
5	S1	Source 1
6	D1	Drain 1

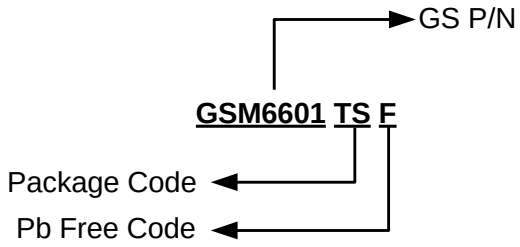


n-channel



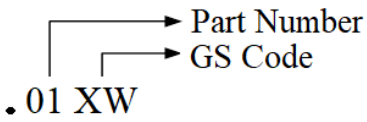
p-channel

Ordering Information



Part Number	Package	Quantity Reel
GSM6601TSF	TSOP-6	3000 PCS

Marking Information



Absolute Maximum Ratings

T_A=25ºC Unless otherwise noted

Symbol	Parameter		Typical		Unit
			N-Channel	P-Channel	
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate –Source Voltage		±12	±12	V
I_D	Continuous Drain Current (Note 1)	T_A=25℃	3.8	-2.3	A
		T_A=70℃	3	-1.8	
I_{DM}	Pulsed Drain Current (Note 2)		16	-15	A
I_S	Continuous Source Current (Diode Conduction) (Note 1,4)		1.1	-1.1	A
P_D	Power Dissipation (Note 3)	T_A=25℃	1.1		W
		T_A=70℃	0.8		
T_J	Operating Junction Temperature		-55/150		℃
T_{STG}	Storage Temperature Range		-55/150		℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient (Note 1)		110		℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case (Note 1)		70		℃/W

Electrical Characteristics (N-Channel)

(T_A=25ºC unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.4		1.2	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V T_J=25ºC			1	uA
		V_{DS}=24V, V_{GS}=0V, T_J=55ºC			5	
$R_{DS(on)}$	Drain-Source On-Resistance (Note 2)	V_{GS}=10V, I_D=3.4A		40	55	mΩ
		V_{GS}=4.5V, I_D=3.0A		45	65	
		V_{GS}=2.5V, I_D=2.0A		60	85	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3.4A		6		S
V_{SD}	Diode Forward Voltage (Note 2)	I_S=1.0A, V_{GS}=0V			1.2	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V,f=1MHz		662		pF
C_{oss}	Output Capacitance			52		
C_{rss}	Reverse Transfer Capacitance			45		
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=3.0A		8.4		nC
Q_{gs}	Gate-Source Charge			1.6		
Q_{gd}	Gate-Drain Charge			1.8		
$t_{d(on)}$	Turn-On Time	V_{DD}=10V, R_G=3.3Ω, I_D=3.0A, V_{GS}=4.5V		3.2		ns
T_r				41.8		
$t_{d(off)}$	Turn-Off Time			21.2		
T_f				6.4		

Note:

1. The data testing by surface mounting on a 1 inch2 / FR4 board/ 2 OZ copper.
2. The data testing by pulsed, pulse width≦ 300us, duty cycle≦ 2%
3. The power dissipation is limited by 150ºC junction temperature
4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Electrical Characteristics (P-Channel)

(T_A=25ºC unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.4		-1.2	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V T_J=25ºC			-1	uA
		V_{DS}=-24V, V_{GS}=0V, T_J=55ºC			-5	
$R_{DS(on)}$	Drain-Source On-Resistance (Note 2)	V_{GS}=-10.0V, I_D=-2.3A		90	115	mΩ
		V_{GS}=-4.5V, I_D=-2.0A		102	145	
		V_{GS}=-2.5V, I_D=-1.0A		136	200	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-2.3A		5.3		S
V_{SD}	Diode Forward Voltage (Note 2)	I_S=-1.0A, V_{GS}=0V			-1.2	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		710		pF
C_{oss}	Output Capacitance			79		
C_{rss}	Reverse Transfer Capacitance			57		
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-2.0A		8.1		nC
Q_{gs}	Gate-Source Charge			1.2		
Q_{gd}	Gate-Drain Charge			2.1		
$t_{d(on)}$	Turn-On Time	V_{DD}=-10V, I_D=-2.0A, V_{GS}=-4.5V, R_G=3.3Ω		4		ns
T_r				33.2		
$t_{d(off)}$	Turn-Off Time			26		
T_f				11.6		

Note:

1. The data testing by surface mounting on a 1 inch^2 / FR4 board/ 2 OZ copper.
2. The data testing by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
3. The power dissipation is limited by 150ºC junction temperature
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics (N-Channel)

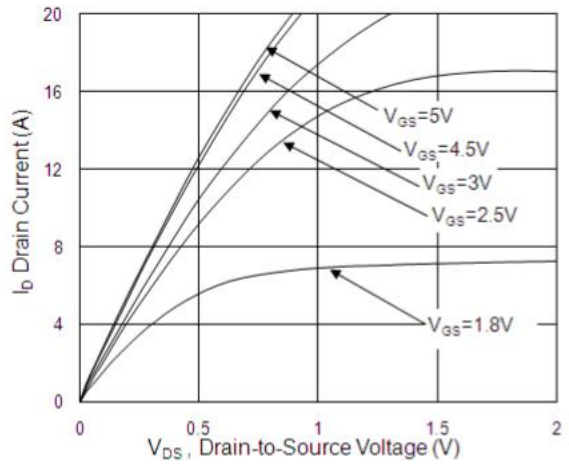


Fig.1 Typical Output Characteristics

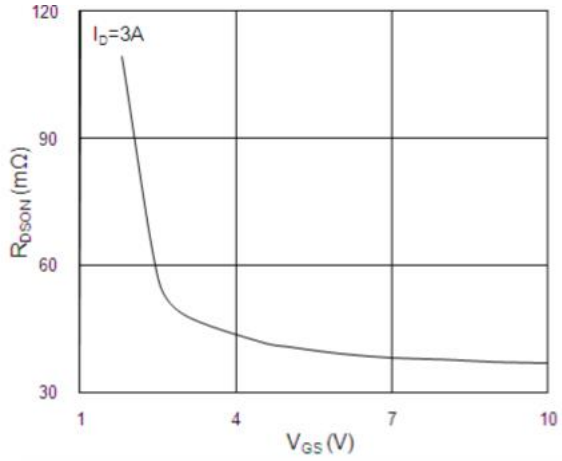


Fig.2 On-Resistance vs.Gate-Source

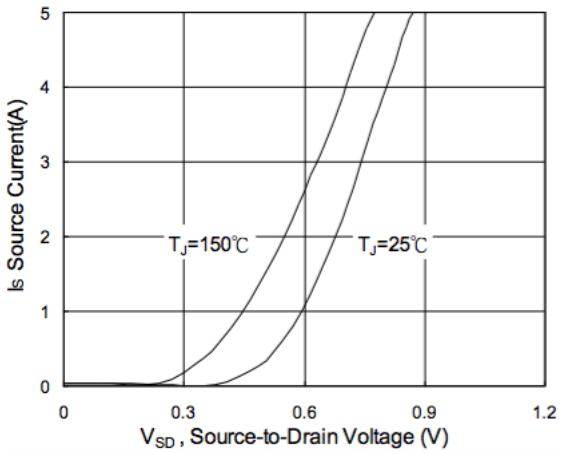


Fig.3 Forward Characteristics of Reverse

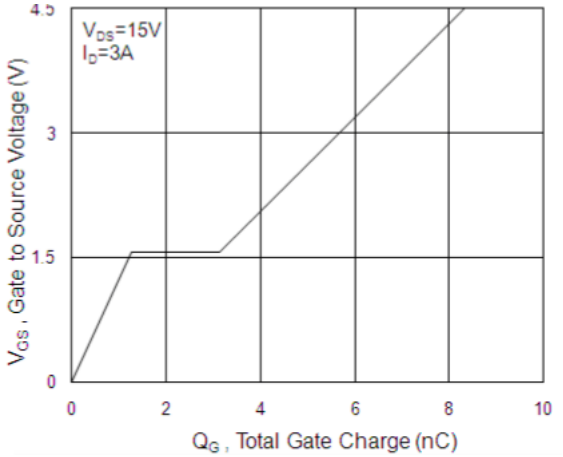


Fig.4 Gate-Charge Characteristics

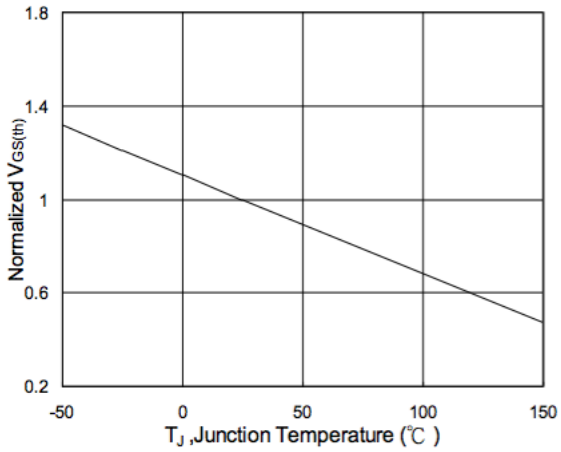


Fig.5 Normalized $V_{GS(th)}$ vs.T_J

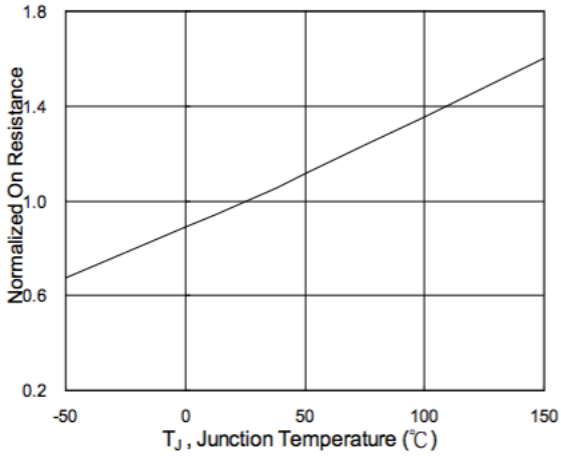


Fig.6 Normalized R_{DSON} vs.T_J

Typical Performance Characteristics (N-Channel Continue)

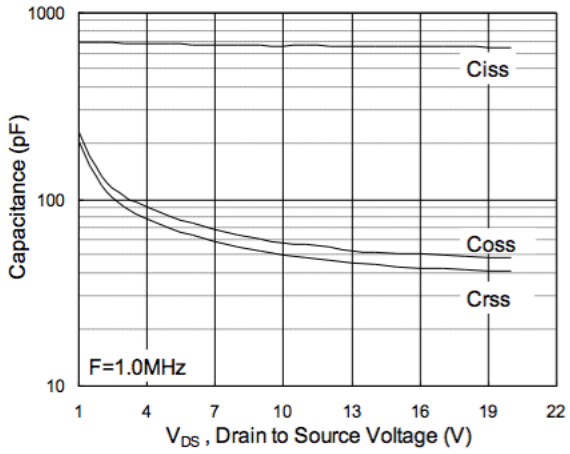


Fig.7 Capacitance

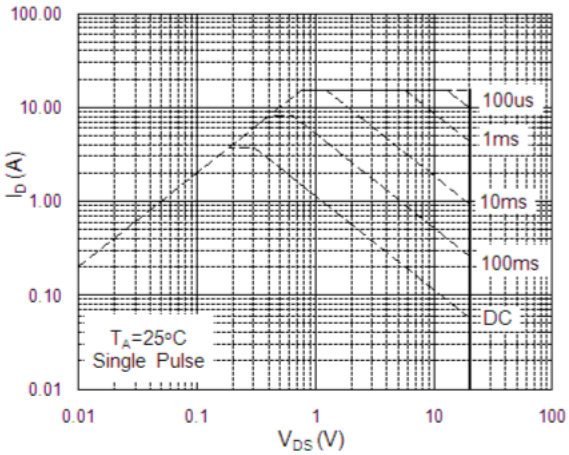


Fig.8 Safe Operating Area

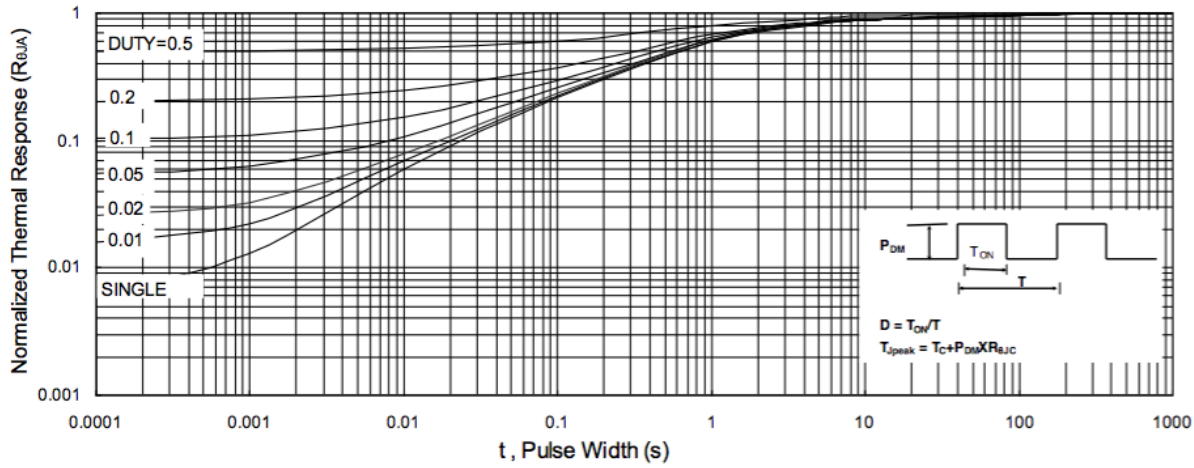


Fig.9 Normalized Maximum Transient Thermal Impedance

Typical Performance Characteristics (P-Channel)

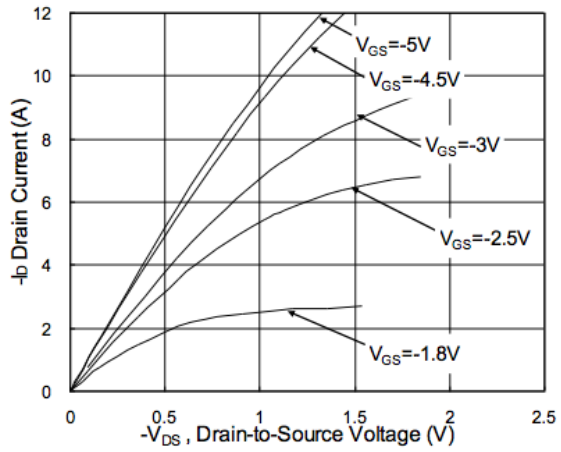


Fig.1 Typical Output Characteristics

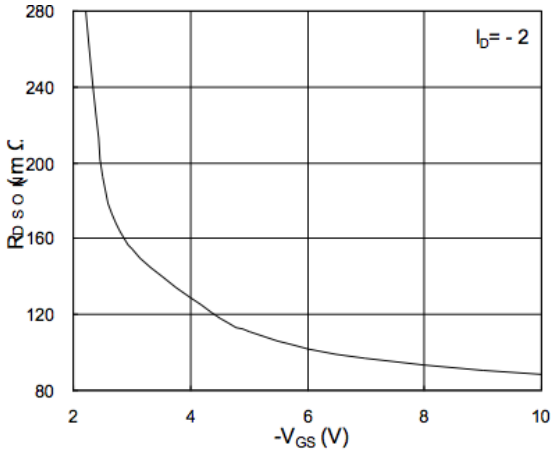


Fig.2 On-Resistance vs.Gate-Source

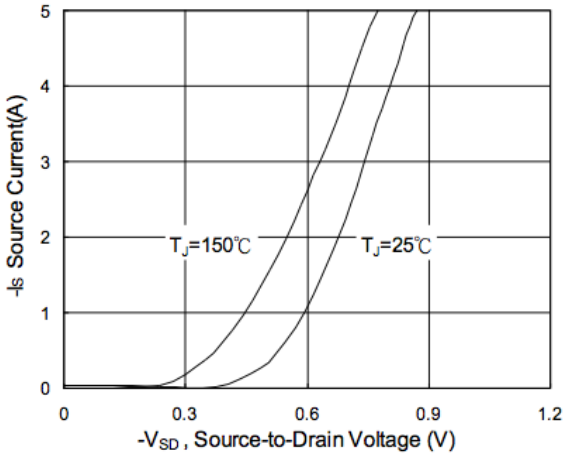


Fig.3 Forward Characteristics of Reverse

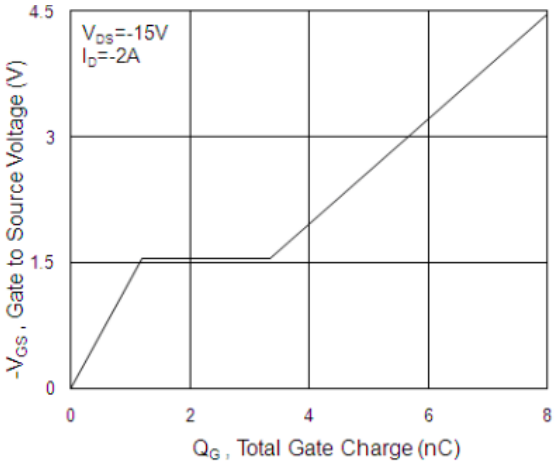


Fig.4 Gate-Charge Characteristics

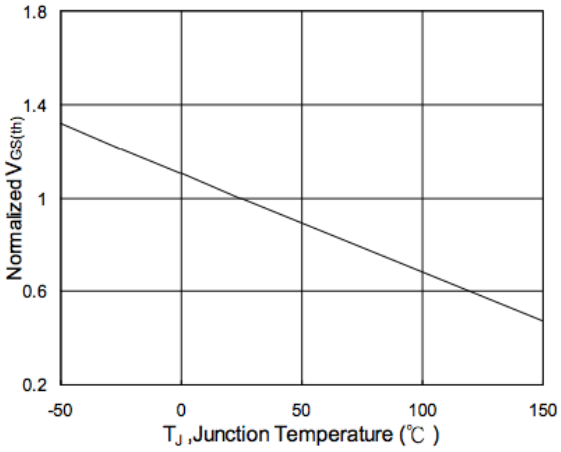


Fig.5 Normalized $V_{GS(th)}$ vs.T_J

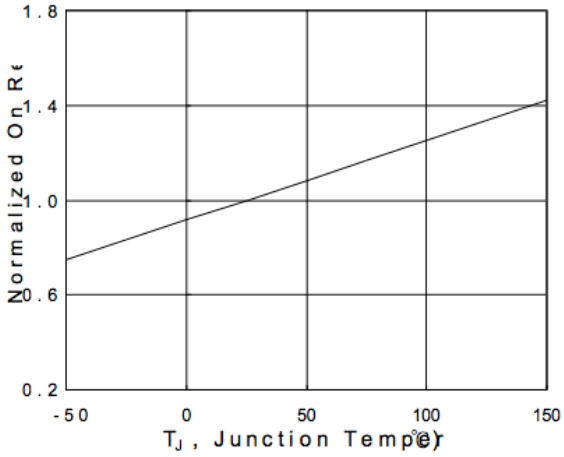


Fig.6 Normalized R_{DSON} vs.T_J

Typical Performance Characteristics (P-Channel Continue)

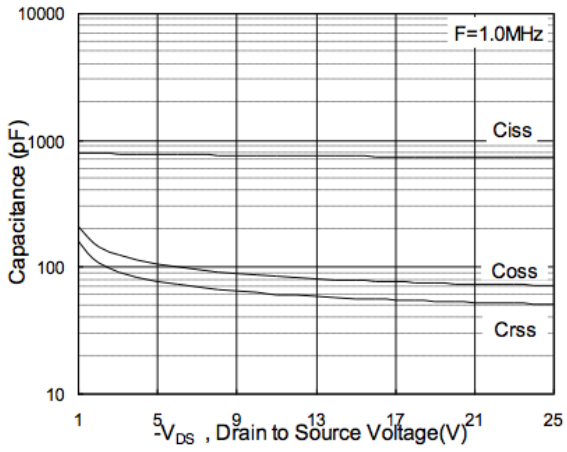


Fig.7 Capacitance

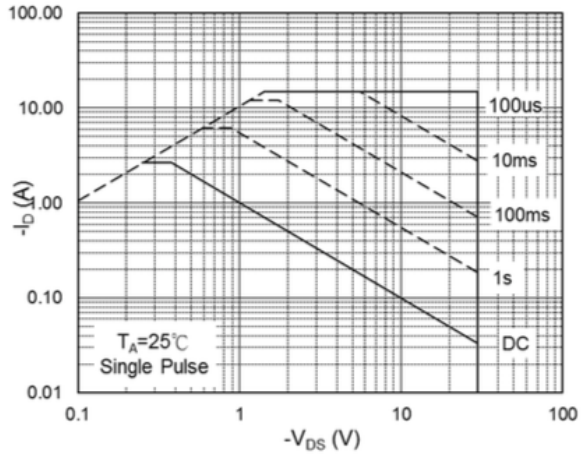


Fig.8 Safe Operating Area

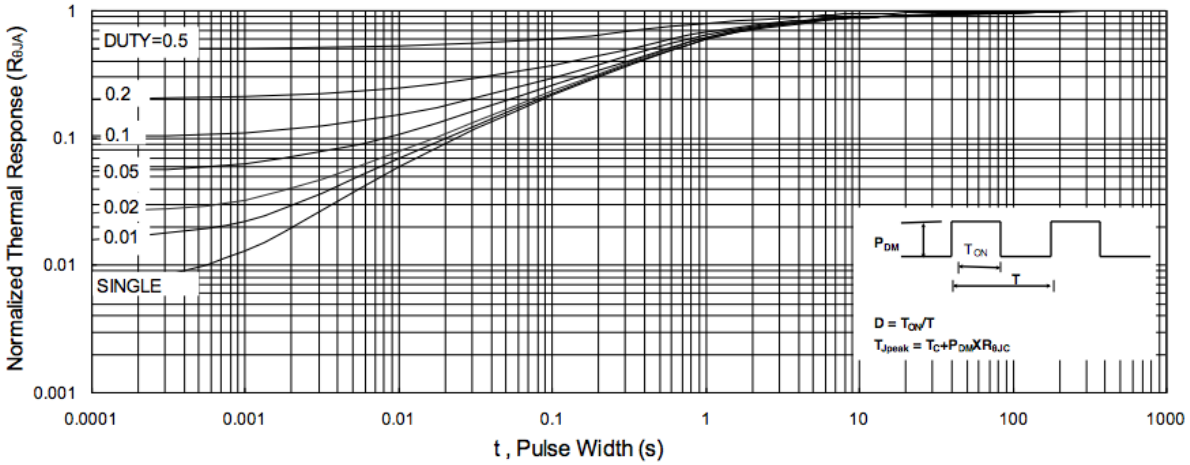
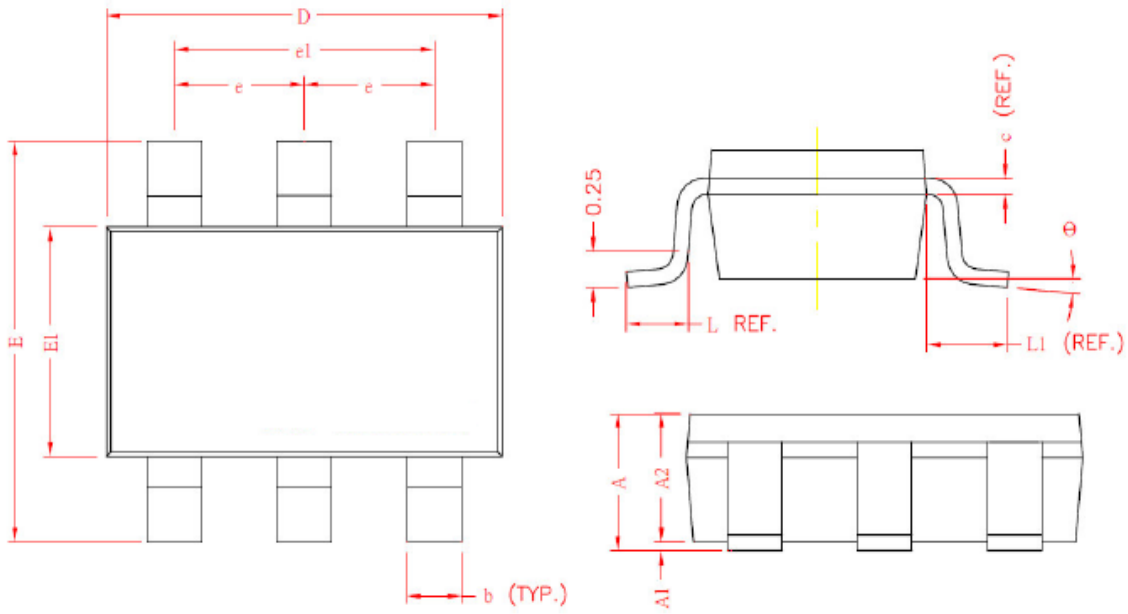


Fig.9 Normalized Maximum Transient Thermal Impedance

TSOP-6 PLASTIC PACKAGE



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0.00	0.10	0.000	0.004
A2	0.70	1.35	0.028	0.053
c	0.12 (REF)		0.005 (REF)	
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
L	0.45 (REF)		0.018 (REF)	
L1	0.60 (REF)		0.024 (REF)	
θ	0°	10°	0°	10°
b	0.30	0.50	0.012	0.020
e	0.95 (REF)		0.037 (REF)	
e1	1.90 (REF)		0.075 (REF)	

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