# GSM3825EX7F

# 30V P-Channel Enhancement Mode MOSFET

#### **Product Description**

GSM3825EX7F, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

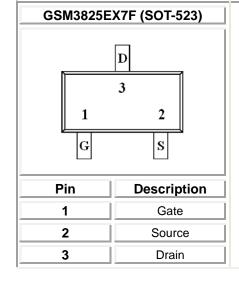
#### **Features**

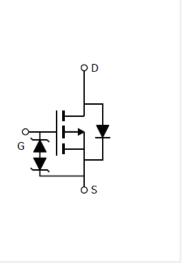
- $\begin{array}{lll} & -30 \text{V/-0.27A}, \; R_{DS(ON)} \!\!=\!\! 2500 m \Omega @V_{GS} \!\!=\!\! -4.5 \text{V} \\ & R_{DS(ON)} \!\!=\!\! 2900 m \Omega @V_{GS} \!\!=\!\! -2.5 \text{V} \\ & R_{DS(ON)} \!\!=\!\! 5000 m \Omega @V_{GS} \!\!=\!\! -1.8 \text{V} \end{array}$
- Low-Voltage Operation
- High-Speed Circuits
- ESD Protection
- SOT-523 package design

#### **Applications**

- Drivers : Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

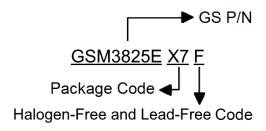
#### **Packages & Pin Assignments**





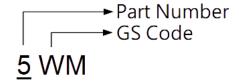


### **Ordering Information**



Part Number	Package Quantity Reel	
GSM3825EX7F	SOT-523	3000 PCS

### **Marking Information**



#### **Absolute Maximum Ratings**

(T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter		Typical	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		-30	V	
Vgss	Gate-Source Voltage		±10	V	
	Continuous Drain Current <sup>2</sup>	T <sub>A</sub> =25°C	-0.27		
l <sub>D</sub>		T <sub>A</sub> =70°C	-0.22	Α	
I <sub>DM</sub>	Pulsed Drain Current		-1.2	Α	
D.	Power Dissipation <sup>2</sup>	T <sub>A</sub> =25°C	0.28	14/	
P <sub>D</sub>		T <sub>A</sub> =70°C	0.18	W	
Reja	Thermal Resistance Junction to ambient <sup>1</sup>		530	°C/W	
R <sub>θJA</sub>	Thermal Resistance Junction to ambient <sup>2</sup>		450	°C/W	
TJ	Operating Junction Temperature Range		-55 to +150	°C	
T <sub>STG</sub>	Storage Temperature Range		-55 to +150	°C	

Note1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. Note2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.



## **Electrical Characteristics**

(T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
		Static					
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V	
$V_{\text{GS(th)}}$	Gate Threshold Voltage V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA -0.4			-1.0			
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±10	uA	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.5A		1.45	2.5		
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.2A		1.85	2.9	Ω	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-0.1A		2.4	5.0		
<b>g</b> FS	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.25A		610		mS	
V <sub>SD</sub>	Diode Forward Voltage	Is=-0.5A, V <sub>GS</sub> =0V			1.3	V	
		Dynamic					
Qg	Total Gate Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A		1.0			
Qgs	Gate-Source Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-8V,		0.2		nC	
$Q_{gd}$	Gate-Drain Charge	I <sub>D</sub> =-1A		0.1			
C <sub>iss</sub>	Input Capacitance			54			
Coss	Output Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V		10.9		pF	
Crss	Reverse Transfer Capacitance	f=1MHz		5.8			
t <sub>d(on)</sub>	Turn-On Time			3.8			
t <sub>r</sub>	Tuin-On Time	$V_{DD}$ =-10V, R <sub>L</sub> =47 $\Omega$ , I <sub>D</sub> =-0.2A		11			
$t_{d(off)}$	T 0# Time e	$V_{GEN}=-4.5V$ , $R_{G}=10\Omega$		45		ns	
t <sub>f</sub>	Turn-Off Time			20			



#### **Typical Performance Characteristics**

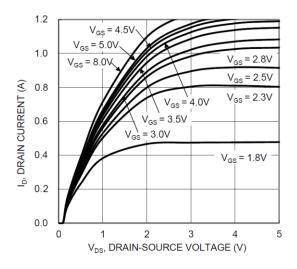


Fig. 1 Typical Output Characteristics

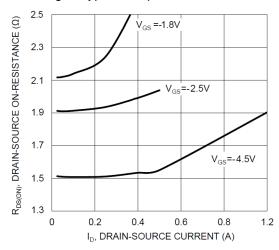


Fig. 3 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$ 

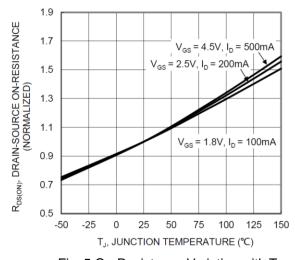


Fig. 5 On-Resistance Variation with T<sub>J</sub>

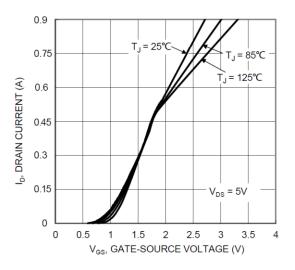


Fig. 2 Typical Transfer Characteristics

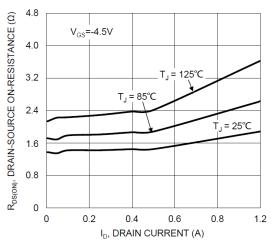


Fig. 4 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_J$ 

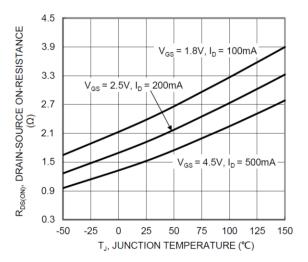
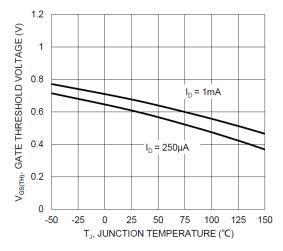


Fig. 6 On-Resistance Variation with T<sub>J</sub>



### **Typical Performance Characteristics (continue)**



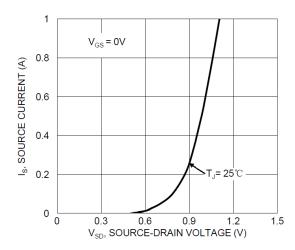
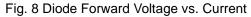
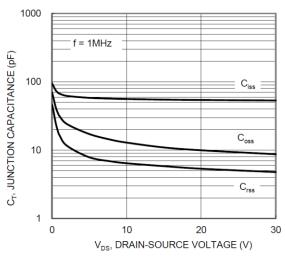


Fig. 7 Gate Threshold Variation vs. TJ





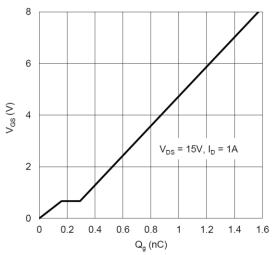


Fig. 9 Typical Capacitance

Fig. 10 Gate Charge

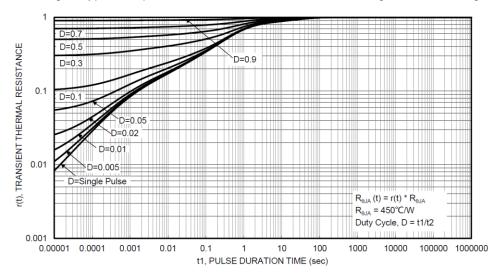
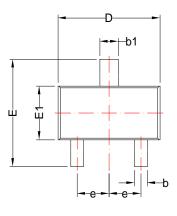


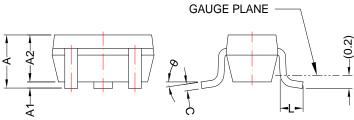
Fig. 11 Transient Thermal Response



## **Package Dimension**

# **SOT-523**





DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH, TIE BAR BURRS  $\,^{,}$  GATE BURRS  $\,^{,}$  AND INTERLEAD FLASH, NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY

		Dimensions		
Corrects and	Millin	neters	Inc	hes
Symbol	Min	Max	Min	Max
Α	0.60	0.95	0.024	0.037
<b>A</b> 1	0.00	0.10	0.000	0.004
A2	0.60	0.85	0.024	0.033
b	0.15	0.30	0.006	0.012
b1	0.25	0.40	0.010	0.016
С	0.08	0.25	0.003	0.010
D	1.40	1.80	0.055	0.071
E	1.40	1.80	0.055	0.071
E1	0.70	0.90	0.028	0.035
е	0.50 BSC		0.020	BSC
L	0.26	0.46	0.010	0.018
θ	00	80	00	80



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