# GSM3825ETF

## 30V P-Channel Enhancement Mode MOSFET

### Product Description

GSM3825ETF, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

### Features

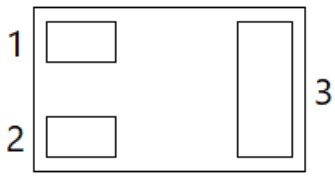
- -30V/-0.5A, $R_{DS(ON)}$=2500mΩ@$V_{GS}$=-4.5V
- -30V/-0.2A, $R_{DS(ON)}$=2900mΩ@$V_{GS}$=-2.5V
- -30V/-0.1A, $R_{DS(ON)}$=5000mΩ@$V_{GS}$=-1.8V
- Low-Voltage Operation
- High-Speed Circuits
- ESD Protection
- DFN1006-3L package design

### Applications

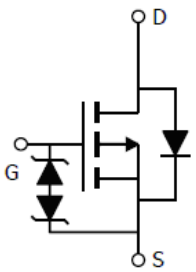
- Drivers : Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

### Packages & Pin Assignments

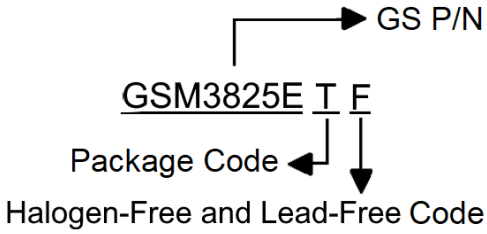
**GSM3825ETF (DFN1006-3L)**




| Pin | Description |
|---|---|
| 1 | Gate |
| 2 | Source |
| 3 | Drain |

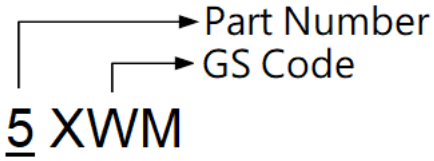


## Ordering Information




| Part Number | Package | Quantity Reel |
|---|---|---|
| GSM3825ETF | DFN1006-3L | 10000 PCS |

## Marking Information




## Absolute Maximum Ratings

($T_A$=25ºC unless otherwise noted)

| Symbol | Parameter | | Typical | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | -30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±10 | V |
| $I_D$ | Continuous Drain Current[1] | $T_A$=25℃ | -0.32 | A |
| | | $T_A$=70℃ | -0.26 | |
| $I_{DM}$ | Pulsed Drain Current | | -1.2 | A |
| $P_D$ | Power Dissipation[1] | $T_A$=25℃ | 0.4 | W |
| $R_{\theta JA}$ | Thermal Resistance Junction to ambient[1] | | 315 | ºC/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to ambient[2] | | 160 | ºC/W |
| $T_J$ | Operating Junction Temperature Range | | -55 to +150 | ºC |
| $T_{STG}$ | Storage Temperature Range | | -55 to +150 | ºC |

Note1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
Note2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

## Electrical Characteristics

($T_A$=25ºC unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=-250uA | -30 | | | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=-250uA | -0.4 | | -1.0 | |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$=0V, $V_{GS}$=±8V | | | ±10 | uA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-24V, $V_{GS}$=0V | | | -1 | uA |
| $R_{DS(on)}$ | Drain-Source On-Resistance | $V_{GS}$=-4.5V, $I_D$=-0.5A | | 1.5 | 2.5 | Ω |
| | | $V_{GS}$=-2.5V, $I_D$=-0.2A | | 1.9 | 2.9 | |
| | | $V_{GS}$=-1.8V, $I_D$=-0.1A | | 2.4 | 5.0 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-10V, $I_D$=-0.5A | | 960 | | mS |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-0.5A, $V_{GS}$=0V | | | 1.3 | V |
| **Dynamic** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{DS}$=-15V, $V_{GS}$=-4.5V, $I_D$=-1A | | 1.0 | | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{DS}$=-15V, $V_{GS}$=-8V, $I_D$=-1A | | 0.2 | | |
| $Q_{gd}$ | Gate-Drain Charge | | | 0.1 | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=-15V, $V_{GS}$=0V f=1MHz | | 54 | | pF |
| $C_{oss}$ | Output Capacitance | | | 10.9 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 5.8 | | |
| $t_{d(on)}$ | Turn-On Time | $V_{DD}$=-10V, $R_L$=47Ω, $I_D$≡-0.2A $V_{GEN}$=-4.5V, $R_G$=10Ω | | 3.8 | | ns |
| $t_r$ | | | | 11 | | |
| $t_{d(off)}$ | Turn-Off Time | | | 45 | | |
| $t_f$ | | | | 20 | | |

## Typical Performance Characteristics

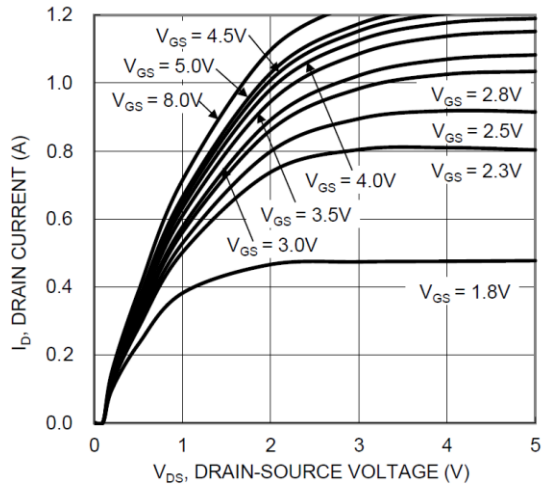



Fig. 1 Typical Output Characteristics

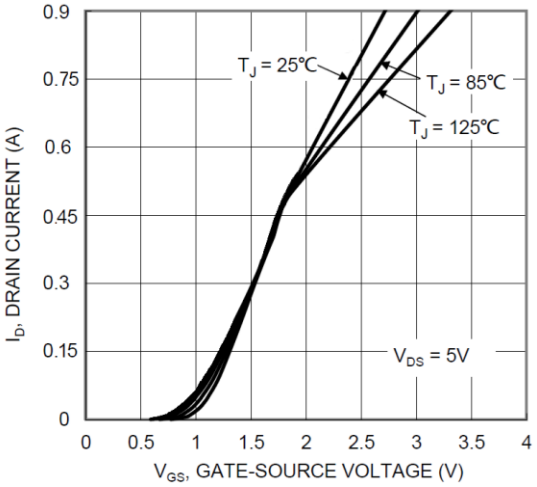



Fig. 2 Typical Transfer Characteristics

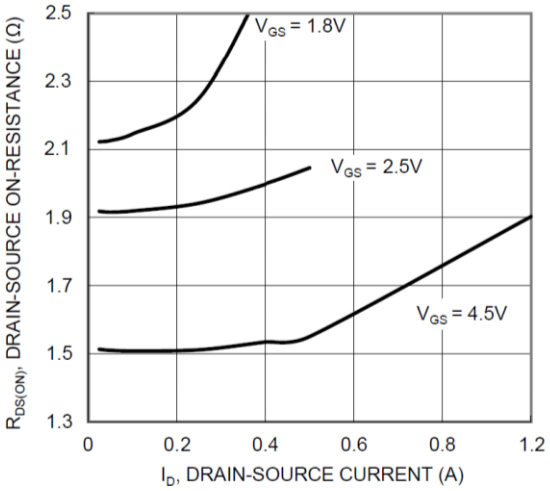



Fig. 3 Typical On-Resistance vs. $I_D$ and $V_{GS}$

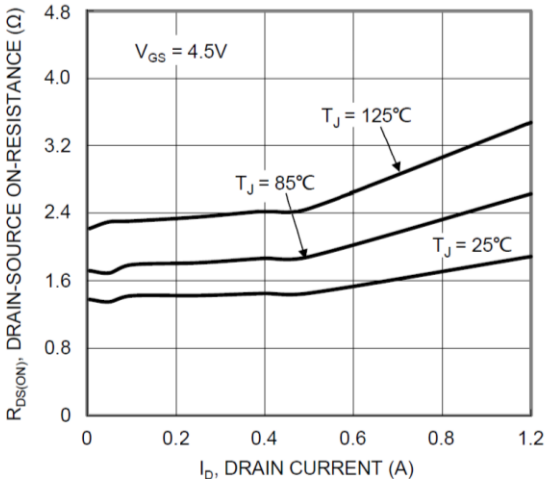



Fig. 4 Typical Drain-Source On-Resistance vs. $I_D$ and $T_J$

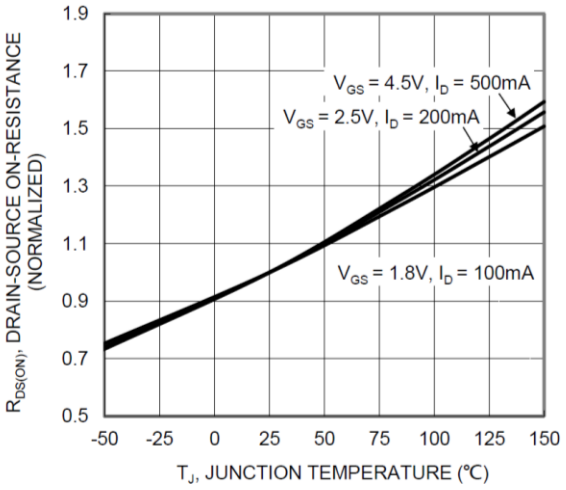



Fig. 5 On-Resistance Variation with $T_J$

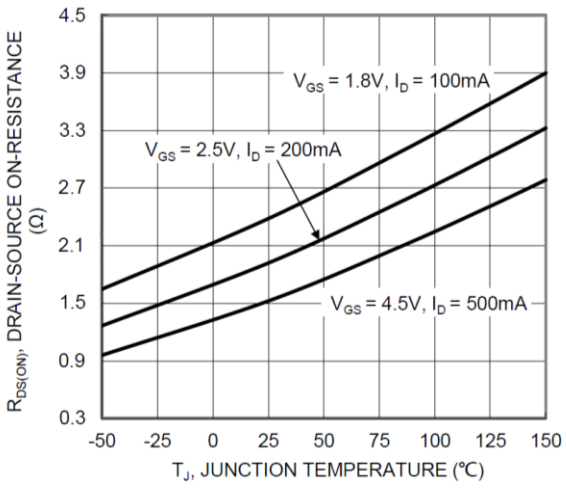



Fig. 6 On-Resistance Variation with $T_J$

## Typical Performance Characteristics **(continue)**

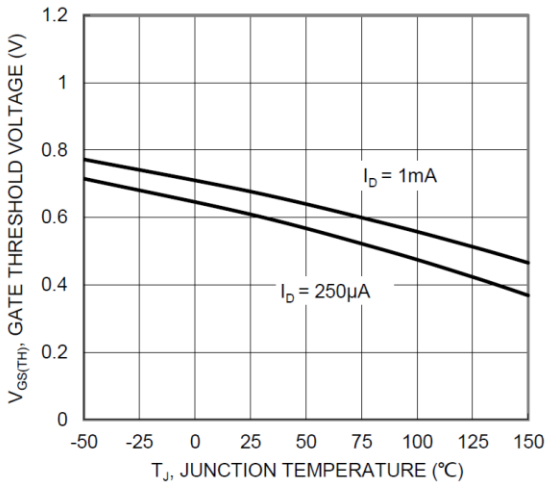



Fig. 7 Gate Threshold Variation vs. $T_A$

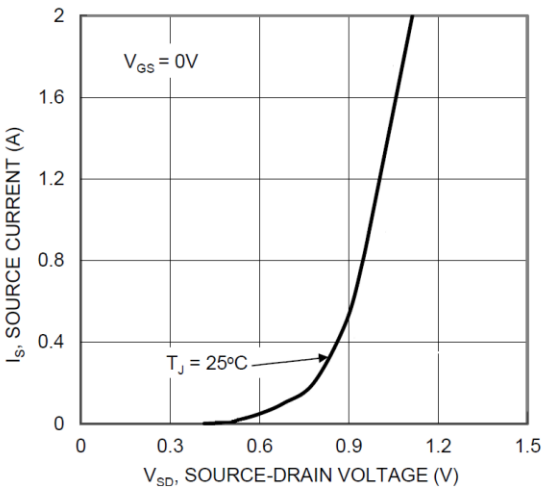



Fig. 8 Diode Forward Voltage vs. Current

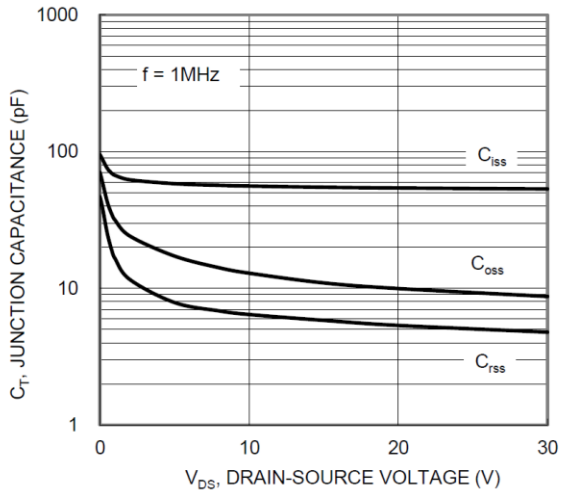



Fig. 9 Typical Capacitance

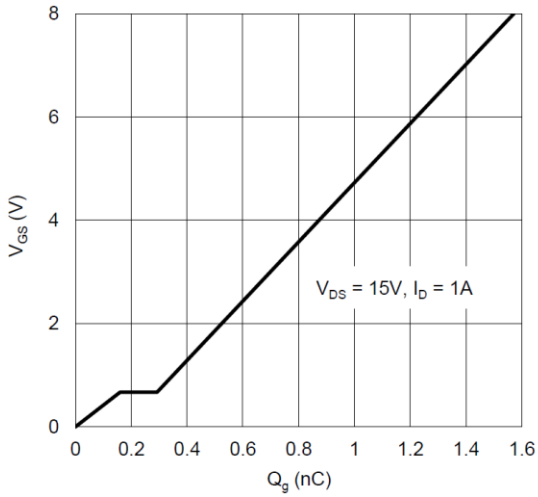



Fig. 10 Gate Charge

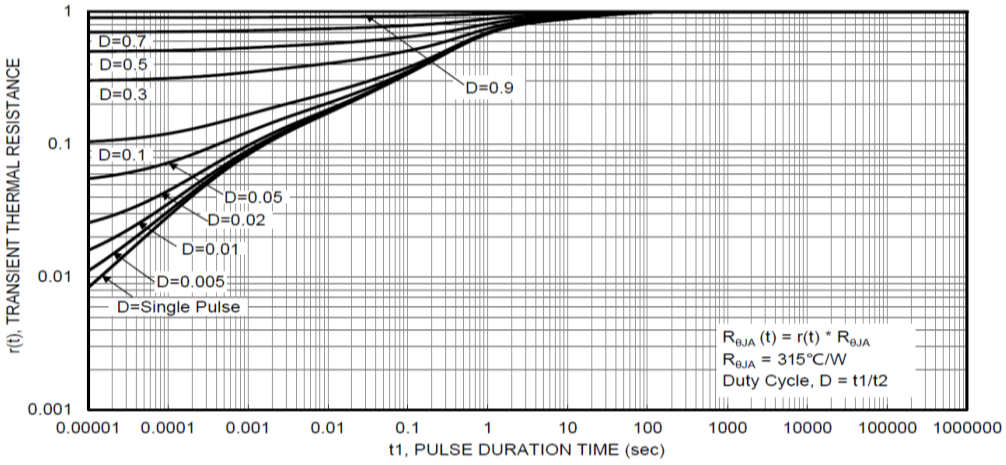
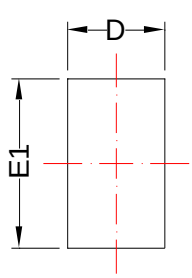
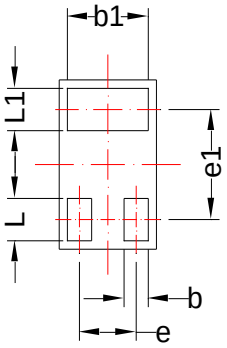



Fig. 11 Transient Thermal Response

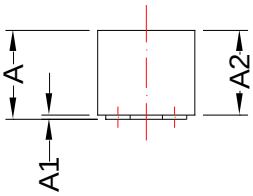
## Package Dimension

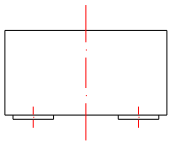
# DFN1006-3L




BACKSIDE VIEW



DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH,TIE BAR BURRS，GATE BURRS，AND INTERLEAD FLASH,NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY

**Dimensions**

| SYMBOL | Millimeters | | Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.45 | 0.60 | 0.018 | 0.024 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A2 | 0.40 | 0.60 | 0.016 | 0.024 |
| b | 0.10 | 0.20 | 0.004 | 0.008 |
| b1 | 0.45 | 0.55 | 0.018 | 0.022 |
| D | 0.55 | 0.65 | 0.022 | 0.026 |
| E1 | 0.95 | 1.05 | 0.037 | 0.041 |
| e | 0.35 BSC | | 0.014 BSC | |
| e1 | 0.65 BSC | | | |
| L | 0.2 | 0.3 | 0.008 | 0.012 |
| L1 | 0.2 | 0.3 | 0.008 | 0.012 |

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