GS5583

1.5MHz, 3A Synchronous Step-Down DC/DC Converter

Product Description

The GS5583 is a high-efficiency, DC-to-DC step-down switching regulators, capable of delivering up to 3.0A of output current. The GS5583 operates from an input voltage range of 2.5V to 6.0V and provides an output voltage from 0.6V to VIN-0.3V, making the device GS5583 ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making GS5583 an ideal green replacement for large power consuming linear regulators.
Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

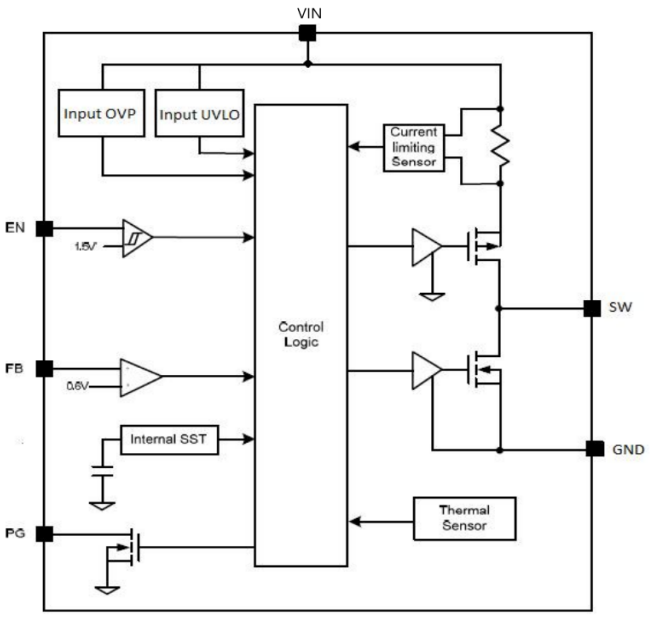
Features

- High Efficiency: Up to 95%
- Capable of Delivering 3.0A
- 1.5MHz Switching Frequency.
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- Internal Compensation and Soft-Start
- Current Mode control
- 0.6V Reference for Low Output voltages
- Logic Control Shutdown (IQ<1uA)
- Input Over Voltage Protection
- Short Circuit Protection
- Thermal shutdown and UVLO
- Power good indicator
- Available in SOT23-6 package

Applications

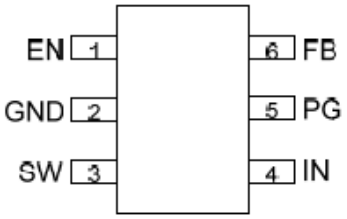
- Digital Cameras
- Set top boxes
- Wireless and DSL Modems
- USB supplied Devices in Notebooks
- Portable Devices

Block Diagram



Packages & Pin Assignments

GS5583RF
SOT23-6L(Top View)



Symbol	Pin(SOT23-6L)	Function
EN	1	Enable pin for the IC. Drive the pin to high to enable the part, and low to disable
GND	2	Ground pin.
SW	3	Inductor connection. Connect an inductor between SW and the regulator output.
IN	4	Power Supply Input Pin. Must be closely decoupled to GND with at least 22uF ceramic cap.
PG	5	Power good indicator. When the output voltage is below 90% of regulation point, It becomes open drain low, otherwise high. Connect this pin to IN by a 1MΩ pull-up resistor.
FB	6	Feedback input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and Vin.

Typical Application Circuit

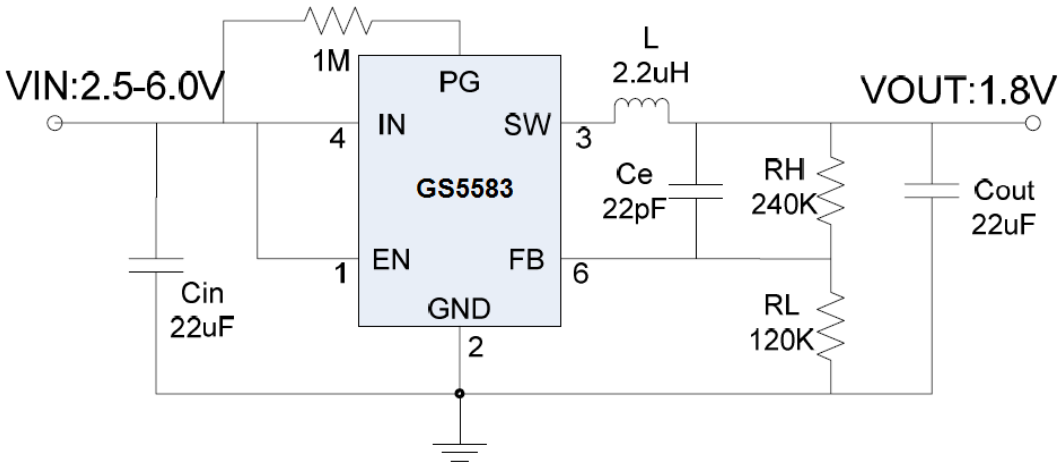
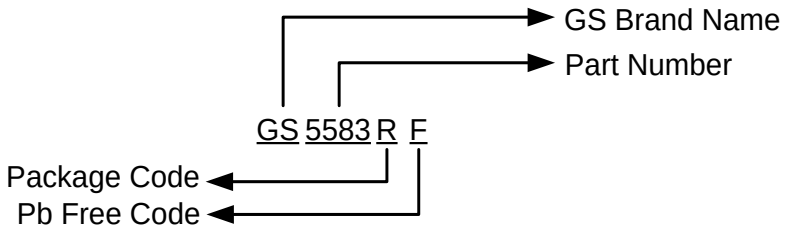


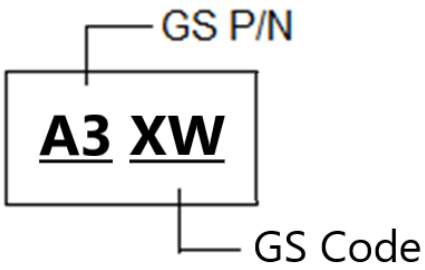
Figure1. GS5583 Adjustable Output Voltage Regulator

Ordering Information



Part Number	Package	Quantity
GS5583RF	SOT23-6L	3000 PCS

Marking Information



Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{IN}	Input Supply Voltage	6.5	V
Tj	Junction Temperature (Note 2)	150	°C
T_A	Operating Temperature Range	-40 to +85	°C
P_D	Power Dissipation	0.4	W
T_{OPT}	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-40 to +150	°C
T_{LEAD}	Lead Temperature(Soldering,10s)	260	°C

Electrical Characteristics

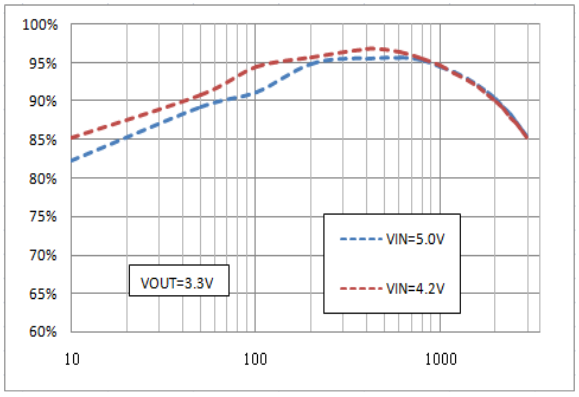
V_{IN} = V_{EN} = 5V, L = 2.2uH, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	-	2.5	-	6.0	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising	-	-	2.5	V
V_{OVP}	Over Voltage Threshold		-	7.1	-	V
V_{HYS}	OVP Hysteresis		-	0.3	-	V
I_Q	Input DC Supply Current	I_{LOAD}=0mA (Note 4)	-	40	-	μA
I_{SHDN}	Input DC Supply Current (Shutdown Mode)	V_{EN}=0V, V_{IN}=4.2V (Note 4)	-	-	1	
V_{FB}	Regulated Feedback Voltage		0.588	0.600	0.612	V
I_{FB}	Feedback Leakage Current		-	0.1	0.4	uA
V_{ENH}	EN Input High Voltage	-	1.5	-	-	V
V_{ENL}	EN Input Low Voltage	-	-	-	0.4	V
I_{EN}	EN Leakage Current	-	-	-	1	μA
I_{SW}	SW Leakage Current	V_{EN}=0V,V_{IN}=Vsw=5V	-	-	1	μA
$R_{DS(ON)H}$	On Resistance of PMOS		-	110	-	mΩ
$R_{DS(ON)L}$	ON Resistance of NMOS		-	80	-	
I_{PK}	Peak Current Limit	-	4	-	-	A
T_{SS}	Soft-Start Time		-	350	-	us
F_{OSC}	Oscillation Frequency		-	1.5	-	MHz

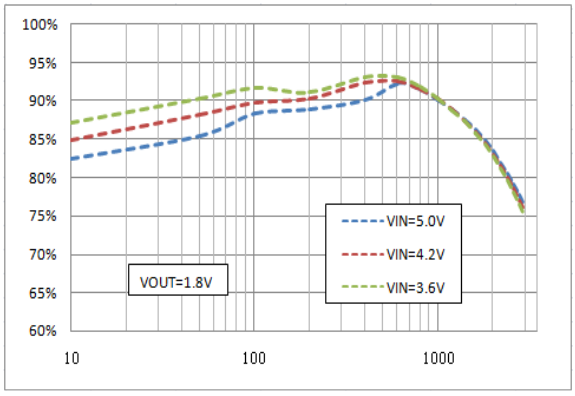
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D) \times (\theta_{JA})$.
Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Typical Performance Characteristics

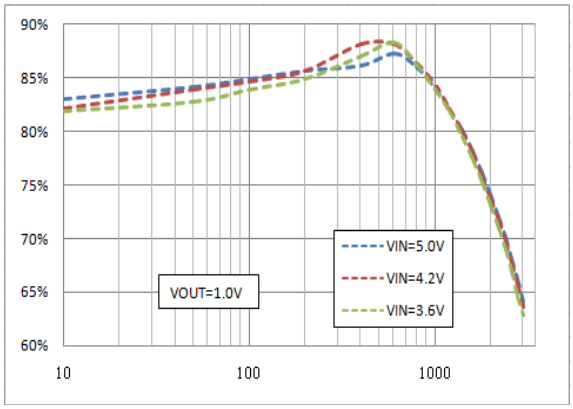
CIN=22μF, COUT=22μF, L=2.2μH, Ce=22pF, Tested under TA=25°C, unless otherwise specified



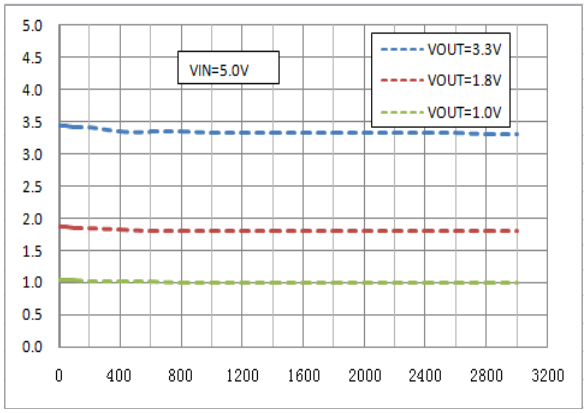
Efficiency vs. Load Current



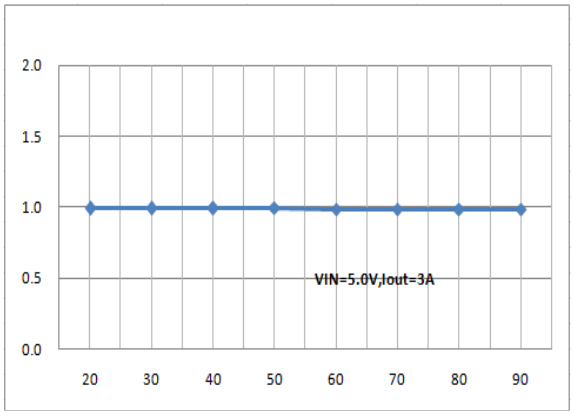
Efficiency vs. Load Current



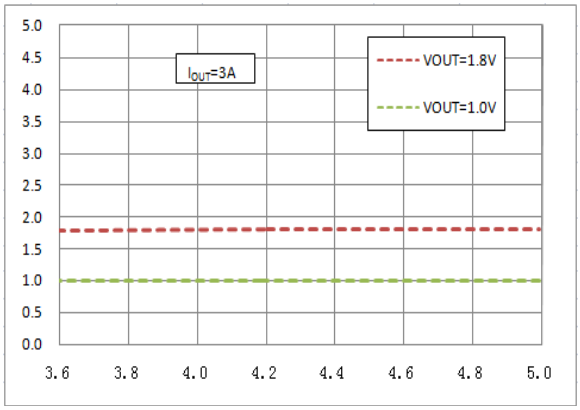
Efficiency vs. Load Current



Output Voltage vs. Output Current



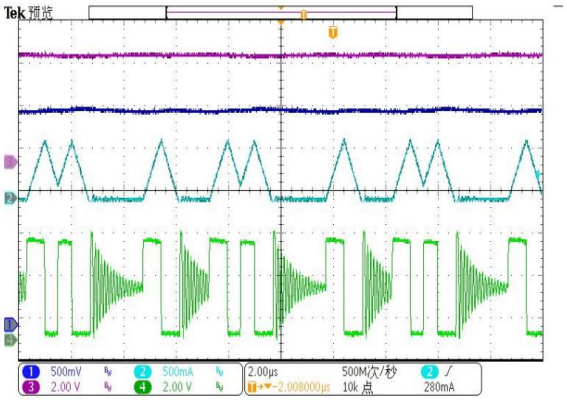
Operation Temperature vs. Output Voltage



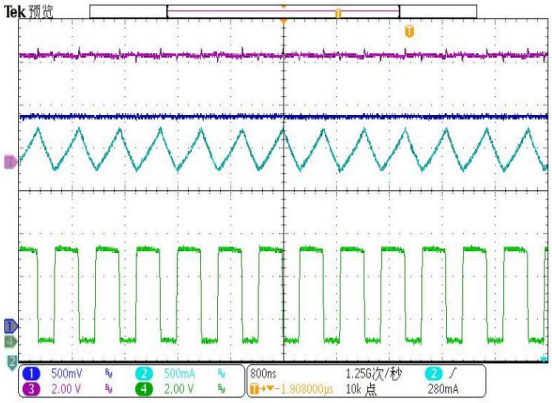
Input Voltage vs. Output Voltage

Typical Performance Characteristics

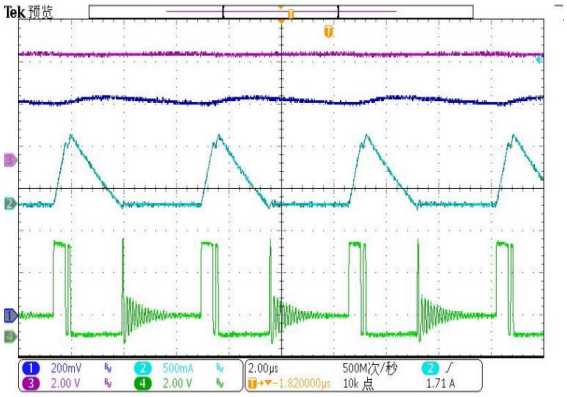
VIN=5.0V, VOUT=2.5V I_{OUT}=200mA



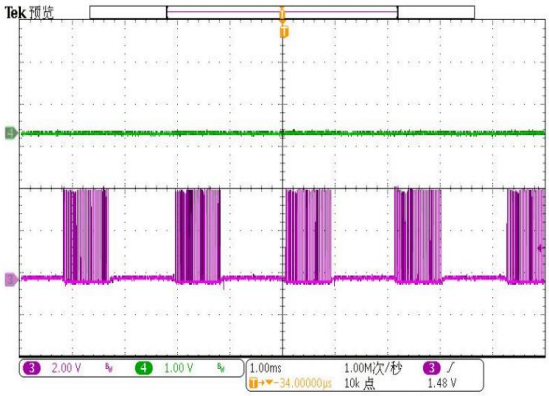
VIN=5.0V, VOUT=2.5V I_{OUT}=2.5A



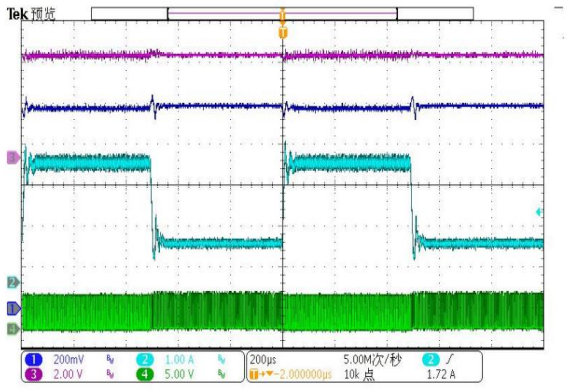
VIN=5.0V, VOUT=1.0V I_{OUT}=200mA



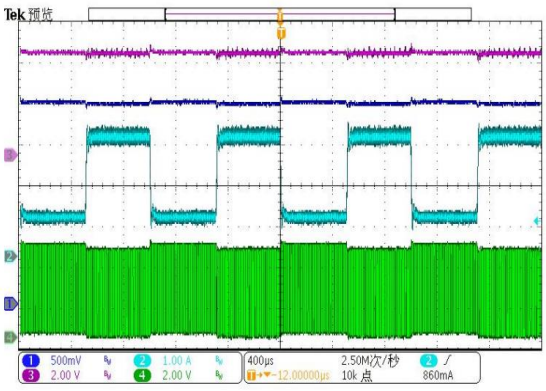
VOUT to GND Short, SW Waveform



VIN=5.0V, VOUT=1.0V I_{OUT}=1A-2.5A
Load Transition



VIN=5.0V, VOUT=2.5V I_{OUT}=1A-2.5A
Load Transition



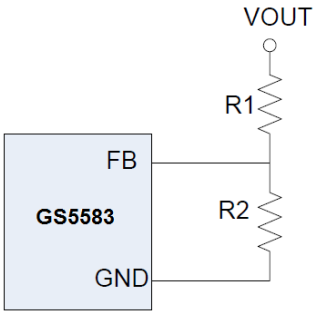
Applications Information

Setting the Output Voltage

Output voltages are set by external resistors. The FB threshold voltage (VFB) is 0.6V.

$$V_{OUT}=0.6Vx(1+\frac{R1}{R2})$$

Set R2 to 100K, then R1 can be easily derived from the above equation



Output Capacitor Selection

The output capacitor is selected to handle the output ripple noise requirements, both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF Capacitance.

Input Capacitor Selection

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

This formula has a maximum at VIN=2V_{OUT} condition, where ICIN_RMS=I_{OUT}/2. This simple worst-case condition is commonly used for the DC-DC design.

With the maximum load current at 3.0A, A typical X5R or better grade ceramic capacitor with 6.3V rating and more than 1pcs 22uF capacitor can handle this ripple current well. To minimize the potential noise problem, ceramics ceramic capacitor should really be placed close to IN and GND pins. Care should be taken to minimize the loop area formed by CIN and IN/GND pins.

Inductor Selection

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple to be about 40% of maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where FSW is the switching frequency and IOUT.MAX is the maximum load current.

The GS5583 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Layout Consideration

Layout is critical to achieve clean and stable operation. The switching power stage requires particular attention.

Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible

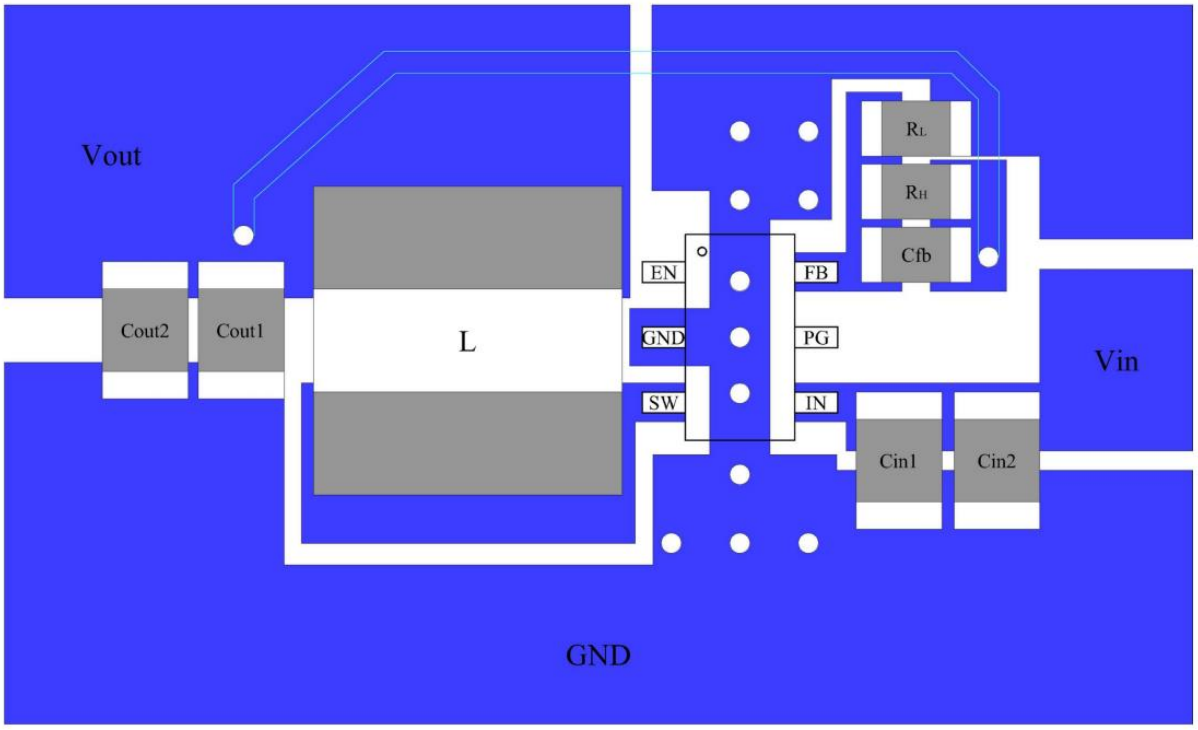
2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.

3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CIN to IN and CIN to GND) short. Avoid vias in the switching paths.

4) If possible, connect IN, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.

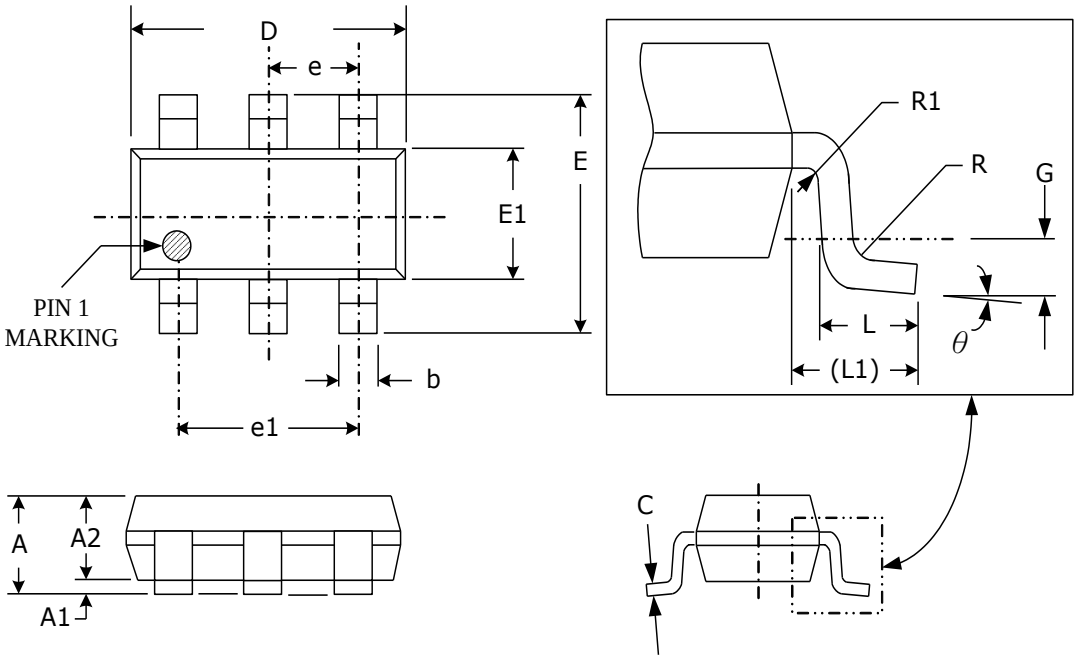
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.

6) Route high-speed switching nodes away from sensitive analog area.



Package Dimension

SOT-23-6L PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	-	1.45	-	.057
A1	0.00	0.15	0	.0059
A2	0.90	1.3	.0354	.0511
b	0.30	0.50	.012	.020
c	0.08	0.20	.003	.008
D	2.90 (TYP)		.114 (TYP)	
E	2.80 (TYP)		.110 (TYP)	
E1	1.60 (TYP)		.063 (TYP)	
e	0.95 (TYP)		.037 (TYP)	
e1	1.90 (TYP)		.075 (TYP)	
L	0.30	0.60	.014	.022
L1	0.60 (TYP)		.024 (TYP)	
R	0.10	-	.004	-
R1	0.10	0.25	.004	.010
G	0.25 (TYP)		.010 (TYP)	
θ	0°	8°	0°	8°

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