GS9121

1.0A/2.0A High-Side Power Switch With Flag

Product Description

The GS9121 serial products are high-side power switch with 80mΩ $R_{DS(ON)}$, available with 1.0A and 2.0A continuous output capability. They are suitable for 3.0V, 3.3V and 5.0V power rail.

GS9121 has enable pin with selectable active high or active low level. It has output discharge feature. It has FLAG pin to indicate the chip status, active low with open drain output once OCP, load short, OTP or OUT-to-IN reverse event is triggered.

GS9121 has lower quiescent current as 25uA making this device ideal for portable battery-operated equipment. Available Package: SOT-23-5L.

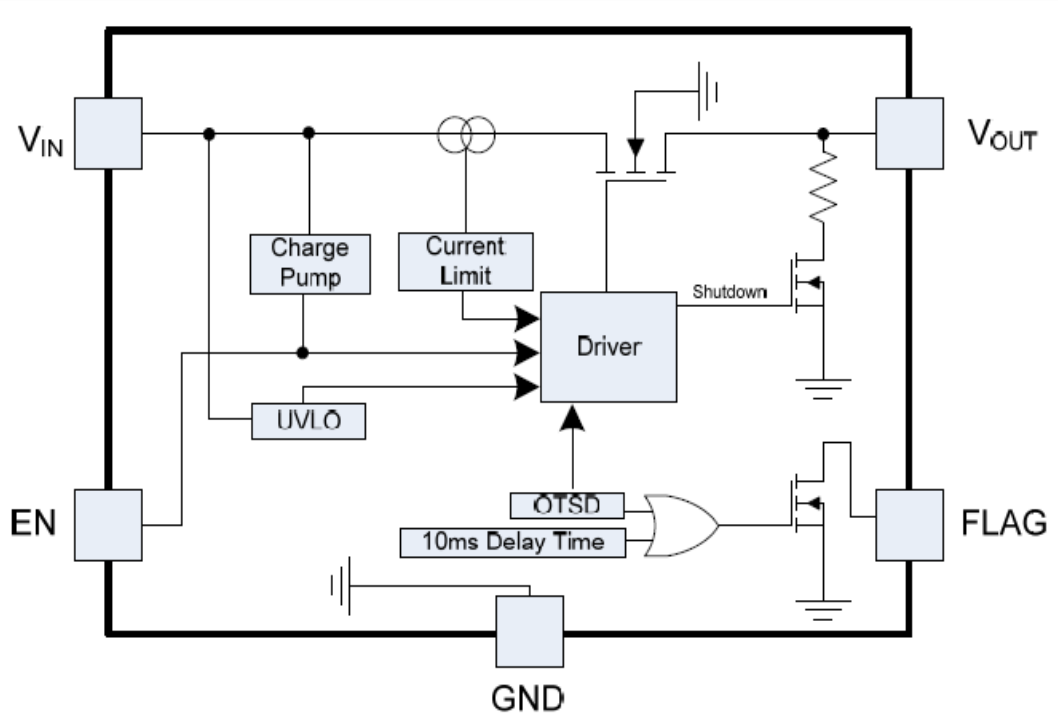
Features

- Integrated high-side Power MOS: 80mΩ(Typ.)
- Operation Voltage: 2.5V to 5.5V
- Compliant to USB Specifications
- Quiescent Current: 25uA(Typ.)
- Shutdown current: 1.0uA(Max.)
- Enable active level selectable: High/Low
- Output discharge feature
- Continuous current: 1.0A/2.0A
- Open-Drain Fault Flag Output
- Hot Plug-In Application (Soft-Start)
- Current Limiting Protection
- Thermal Shutdown Protection
- Reverse Current Flow Blocking (no body diode)
- RoHS Compliant, 100%Pb & Halogen Free
- Device Meets MSL 3 Requirements

Applications

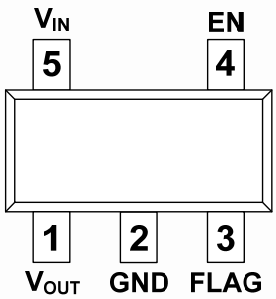
- Notebook & Ultrabook
- Tablet, PAD
- USB 2.0/3.0 Port
- LVDS Port, HDMI Port, DP Port

Block Diagram



Packages & Pin Assignments

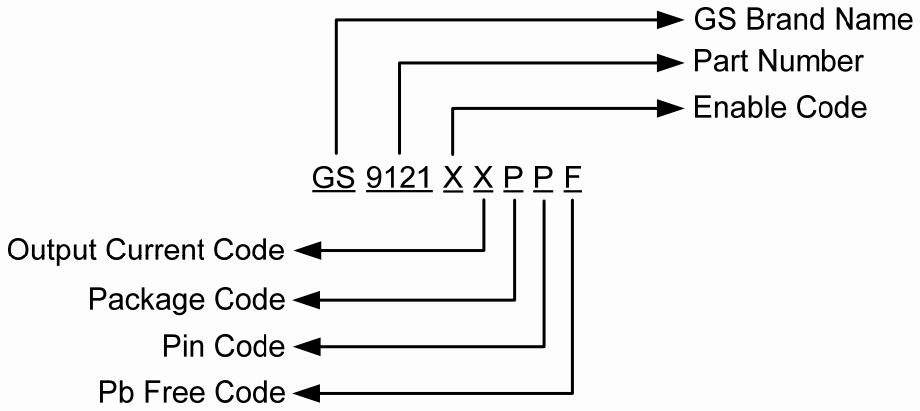
SOT-23-5L (LA Type)



Top View

Pin Name	Description
GND	GND Pin.
V_{IN}	Power supply input pin, using 1.0uF bypass capacitor is enough in most applications, if the distance is long in layout, please using 10uF or larger capacitor close to the chip.
EN	Enable pin, active low or high. Must be set high or low, cannot be left floating.
V_{OUT}	Output pin, using 1.0uF bypass capacitor is enough in most applications, if the distance is long in layout, please using 10uF or larger capacitor close to the chip.
FLAG	Flag output with open drain, active low. Connect a pull-up resistor (10k) to input.

Ordering Information



Part Number	Output Current	Enable	Marking ID	Package
GS9121ABLAF	1.0A	Active High	PBYWG	SOT-23-5L
GS9121BBLAF	1.0A	Active Low	pBYWG	SOT-23-5L
GS9121ADLAF	2.0A	Active High	PEYWG	SOT-23-5L
GS9121BDLAF	2.0A	Active Low	pAYWG	SOT-23-5L

*GS9121Ax, Enable pin-active high, YW=Date code, G=GS code
*GS9121Bx, Enable pin-active low, YW=Date code, G=GS code

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Units
V_{IN}	Input Voltage	6.0	V
V_{EN}	Input Voltage for Enable	-0.3 to 6.0	V
V_{FLG}	Flag Voltage	6.0	V
P_D	Power Dissipation@ T_A=25ºC	0.4	W
T_J	Operating Junction Temperature	125	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC
T_{LEAD}	Lead Temperature(Soldering, 10 sec)	260	ºC
θ_{JA}	Thermal Resistance Junction to Ambient **(Note 2)**	250	ºC/W
θ_{JC}	Thermal Resistance Junction to Case **(Note 2)**	100	ºC/W
T_A	Operating Ambient Temperature Range	-40 to +85	ºC
ESD	Machine Model	200	V
	Human Body Model	4000	V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: Using 2oz dual layer (Top, Bottom) FR4 PCB with 4x4mm^2 cooper as thermal PAD.

Electrical Characteristics (Note 3)

Test Condition: C_{IN}=C_{OUT}=1.0uF, V_{IN}=5.0V, R_L=10Ω, C_L=10uF unless otherwise specified, all limits are test at T_A=25ºC, and bold type is limited at T_A=-40 to 85ºC.

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		-	2.5	-	5.5	V
V_{UVLO}	UVLO Threshold		-	1.3	1.7	-	
V_{UVLOHY}	UVLO Hysteresis		-	-	0.1	-	
I_{SHDN}	Shutdown Quiescent Current		Switch off, V_{OUT}=OPEN	-	0.1	1.0	µA
I_Q	Quiescent Current		Switch on, V_{OUT}=OPEN	-	25	45	µA
$R_{DS(ON)}$	Switch On Resistance		V_{IN}=5V, I_{OUT}=0.5A	-	80	100	mΩ
			V_{IN}=5V, I_{OUT}=1.0A	-	80	100	
I_{LMT}	Current Limit	GS9121xB (1.0A)	Current Ramp (<0.1A/ms) on V_{OUT}	1.2	1.5	1.7	A
		GS9121xD (2.0A)		2.3	2.5	2.7	
I_{SHORT}	Fold-back Short Current	GS9121xB (1.0A)	V_{OUT}=0V	-	0.8	-	A
		GS9121xD (2.0A)		-	1.6	-	
$I_{LEAKAGE}$	Leakage Current (V_{IN} to V_{OUT})		Disable EN pin, V_{OUT}=0V	-	0.5	10	µA
$I_{REVERSE}$	Reverse Current (V_{OUT} to V_{IN})		Disable EN pin, V_{OUT}>V_{IN}	-	0.5	10	µA
V_{ENH}	Enable High Input Threshold		-	2.0	-	-	V
V_{ENL}	Enable Low Input Threshold		-	-	-	0.8	V
I_{EN}	Enable Pin Input Current **(Note 4)**		Force 0V to 5.5V at EN pin	-1.0	-	1.0	µA
R_{PULL}	Output pull-low resistor		with discharge device	-	75	150	Ω
t_{ON}	Output Rising Time		From EN active to output rising 90%, V_{IN}=5.0V, R_L=10Ω	-	0.4	-	ms
t_{FLAG_D}	FLAG response delay time		From OCP trigger to FLAG active	5	10	15	ms
R_{FLAG}	FLAG output resistance		I_{SINK}=1mA	-	20	400	Ω
I_{FLAG_L}	FLAG pin leakage		FLAG disactive, force 5.0V	-	0.01	1.0	µA

Electrical Characteristics (Continue)

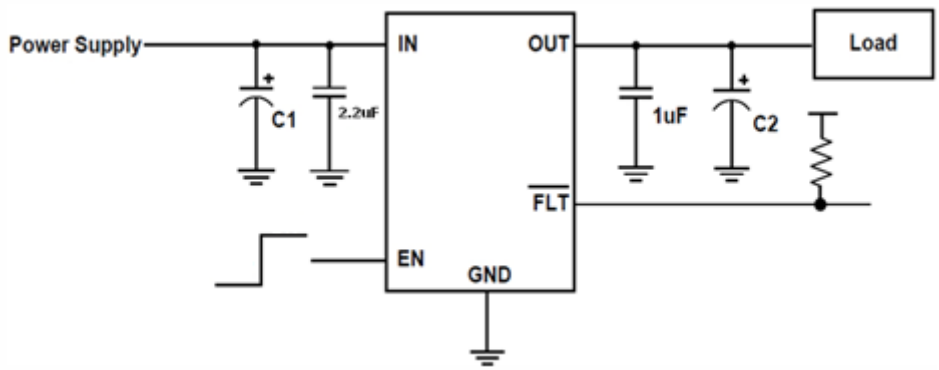
Test Condition: C_{IN}=C_{OUT}=1.0uF, V_{IN}=5.0V, R_L=10Ω, C_L=10uF unless otherwise specified, all limits are test at T_A=25ºC, and bold type is limited at T_A=-40 to 85ºC.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{OTP}	Thermal shutdown temperature	-	-	130	-	ºC
T_{HY}	Thermal shutdown hysteresis	-	-	20	-	ºC

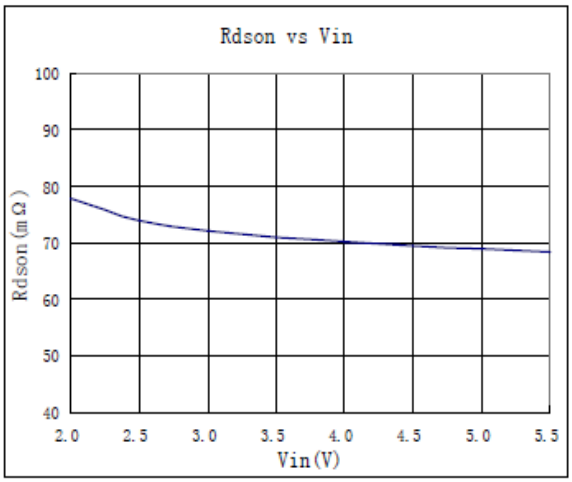
Note 3: All devices are 100% production tested at T_A=+25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested. Parameter is guaranteed by design.

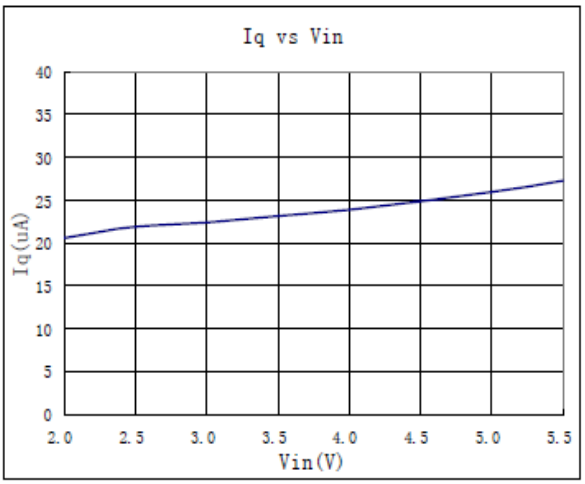
Note 4: No parasitic diode between EN pin and V_{IN} pin.

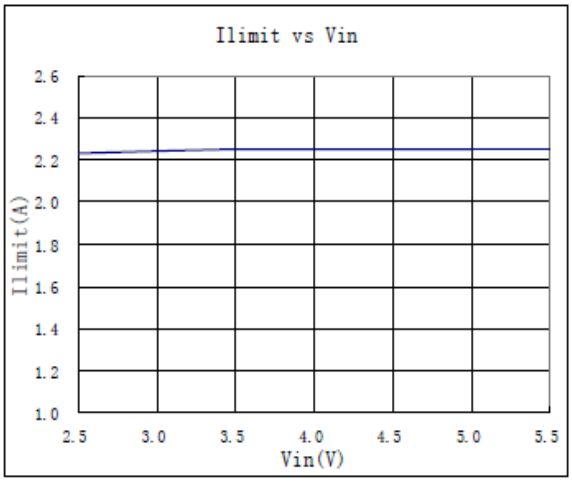
Typical Applications

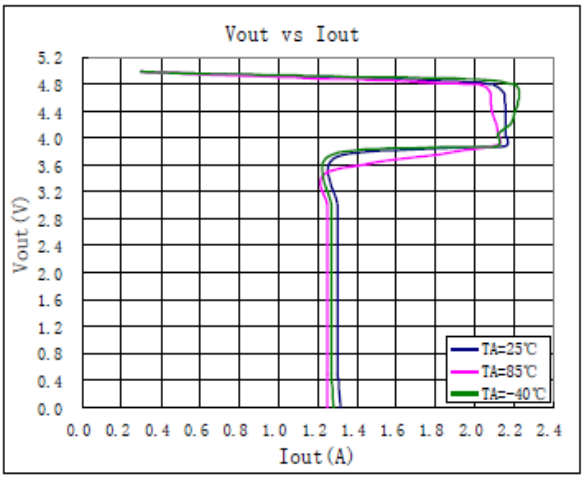


Typical Performance Characteristics









Application Information

Input and Output

IN (input) is the chip power supply connection to the logic circuit and the drain of the power MOSFET. OUT (output) is connected Source of the power MOSFET. In typical application, current flows through the MOSFET channel from IN to OUT.

Thermal Shutdown

Thermal shutdown is employed to protect the device from damage if the die temperature exceeds approximately 130°C. If enabled, the switch automatically restarts when the die temperature falls 20°C. The output and FLG signal will continue to cycle on and off until the device is disabled or the fault is removed.

Power Dissipation

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. It is good design practice to check power dissipation and junction temperature for each application. Begin by determining the $R_{DS(ON)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. Using the highest operating ambient temperature of interest and $R_{DS(ON)}$, the power dissipation per switch can be calculated by:

$P_D = R_{DS(ON)} \times I^2$

Finally, calculate the junction temperature:

$T_J = P_D \times R_{\theta JA} + T_A$

Where:

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

UVLO

Under-voltage lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 1.7V. If input voltage drops below approximately 1.6V, UVLO turns off the MOSFET switch, FLG will be asserted accordingly. Under-voltage detection functions only when the switch is enabled.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 1A/2.1A through the switch of GS9121xB/xD. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

FLAG Function

The FLAG is output to indicate over current, load short, over temperature trigger events. It is active low with open-drain output after 10ms(Typ.) deglitch timeout. The output remains asserted until the over-current condition is removed. Over temperature condition is also reported immediately.

Supply Filtering

In most applications, two 1.0μF bypass capacitors between IN to GND and OUT to GND, close to the chip are strongly recommended to depress supply transients. For long distance layout, larger bypass cap is necessary, like 22uF, 47uF or larger. Without a bypass capacitor, it may cause significant ringing on the input (from supply lead inductance) which could damage the chip during load short. Input transients must not exceed the absolute maximum supply voltage (6.0V) even for a short duration.

Enable Pin

EN pin must be driven logic high or low for a clearly defined input. Floating this pin may cause unpredictable operation. EN pin should not be allowed to go negative voltage comparison to GND. There is no parasitic ESD Diodes between EN pin and IN pin.

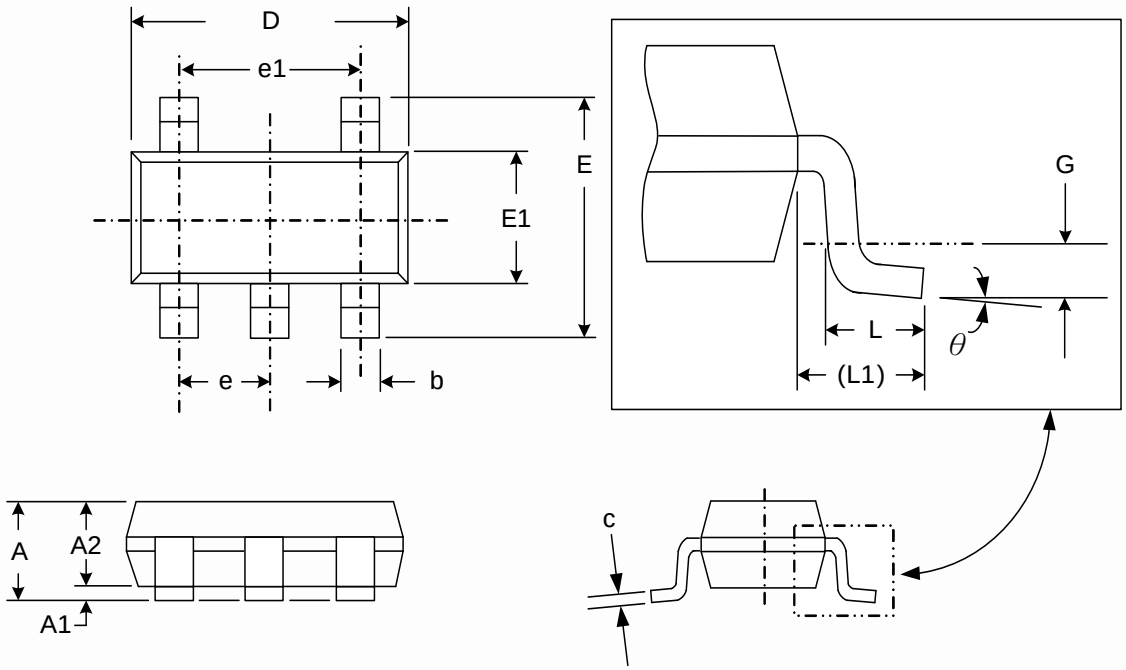
Layout Considerations

For best performance of the GS9121 series, the following guidelines muse be strictly followed:

1. Input and output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.
2. The GND should be connected to a strong ground plane for heat sink.
3. Keep the main current traces as possible as short and wide.

Package Dimension

SOT-23-5L



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.95	1.45	.037	.057
A1	0.05	0.15	.002	.006
A2	0.90	1.30	.035	.051
b	0.30	0.50	.012	.020
c	0.08	0.20	.003	.008
D	2.80	3.00	.110	.118
E	2.60	3.00	.102	.118
E1	1.50	1.70	.059	.067
e	0.95 (TYP)		.037 (TYP)	
e1	1.90 (TYP)		.075 (TYP)	
L	0.35	0.55	.014	.022
L1	0.60 (TYP)		.024 (TYP)	
G	0.25 (TYP)		.010 (TYP)	
θ	0°		0°	8°

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