GS5592

3MHz, 2A Synchronous Step-Down Converter

Product Description

The GS5592 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 2A of output current. The devices operate from an input voltage range of 2.6V to 5.5V and provide output voltages from 0.6V to V_{IN}, making the GS5592 ideal for low voltage power conversions.

Running at a fixed frequency of 3MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. Built-in EMI reduction circuitry makes this converter ideal power supply for RF applications. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

GS5592 is housed in a tiny SOT23-5L and DFN2x2-8L package

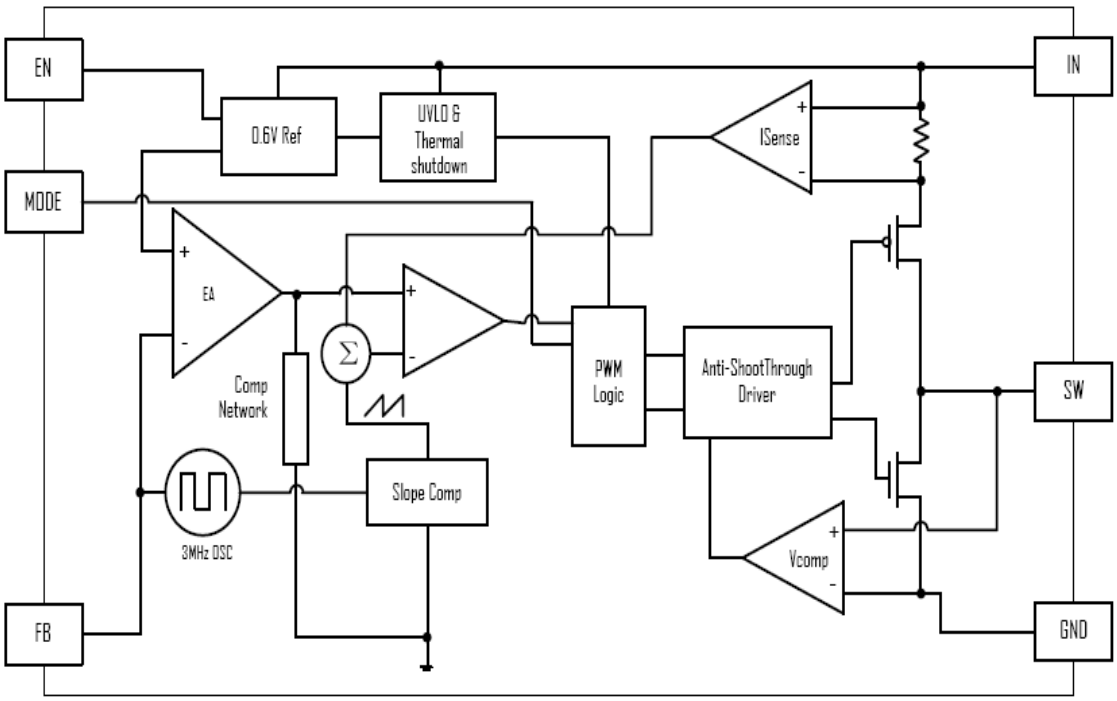
Features

- High Efficiency : Up to 96%
- 3.0MHz Constant Frequency Operation
- 2A Output Current
- Internal Compensation
- Clock Dithering
- Tiny SOT-23-5L and DFN2x2-8L Package
- RoHS Compliant, 100%Pb & Halogen Free

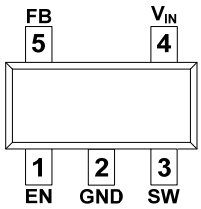
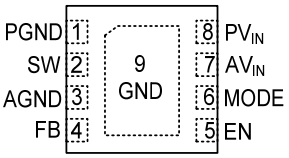
Applications

- USB ports/Hubs
- Portable Devices
- Hot Swaps
- Cell phones
- Tablet PC
- Set Top Boxes

Block Diagram

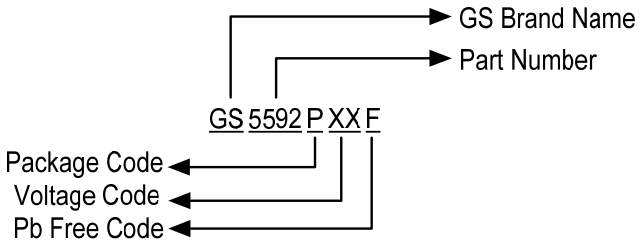


Packages & Pin Assignments

GS5592LAF(SOT-23-5L)	GS5592FAF(DFN2x2-8L)
 (Top View)	 (Top View)

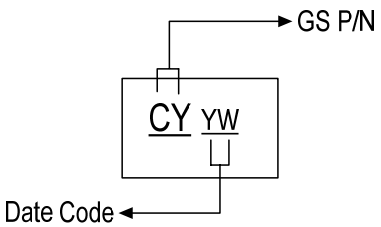
Pin Name	Description
V_{IN}	Supply Voltage. Short to PIN. Bypass with a 10μF ceramic capacitor to GND.
EN	Enable pin for the IC. Drive this pin to high to enable the part, low to disable.
GND	Ground Pin.
SW	Inductor Connection. Connect an inductor Between SW and the regulator output.
FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and V_{IN}.
PGND	Power Ground. Bypass with a 10μF ceramic capacitor to PV_{IN}.
AGND	Analog Ground, Connect to PGND.
MODE	When forced high, the device operates in fixed frequency PWM mode. When forced low, it enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated.
AV_{IN}	Analog Power. Short externally to PV_{IN}.
PV_{IN}	Supply Voltage. Bypass with a 10μF ceramic capacitor to PGND.

Ordering Information



Part Number	Temperature Range	Output Voltage	Package
GS5592LAF	-40°C to 85°C	ADJ	SOT-23-5L
GS5592FAF	-40°C to 85°C	ADJ	DFN2x2-8L

Marking Information



Absolute Maximum Ratings (Note 1)

Symbol	Description		Value	Units
V_{IN}	Supply Voltage		-0.3 to 6.0	V
	Others Voltages		-0.3 to 6.0	V
	SW to Ground Current		Internally Limited	
T_A	Ambient Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-55 to +150	°C
T_{LEAD}	Lead Temperature(Soldering,10s)		260	°C
P_D	Maximum Power Dissipation (T_A=25°C)	SOT-23-5L	0.6	W
		DFN2x2-8L	1.3	

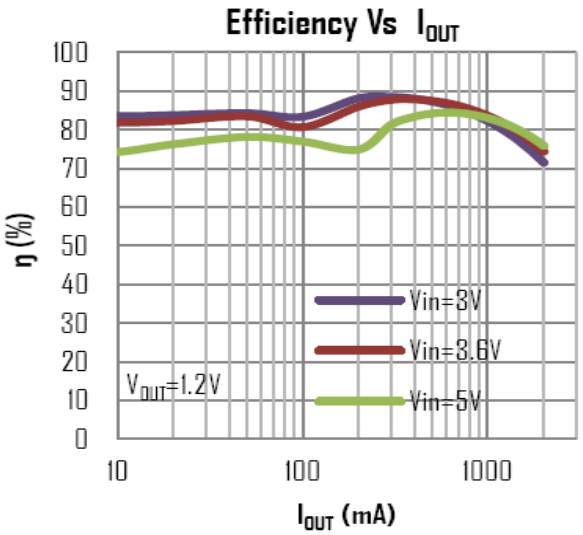
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

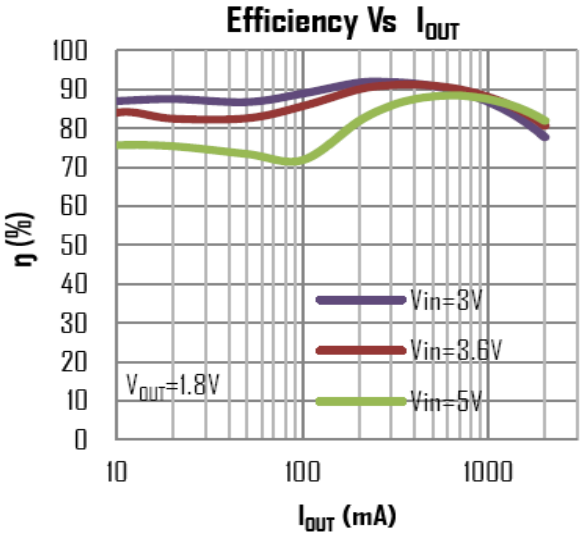
Electrical Characteristics

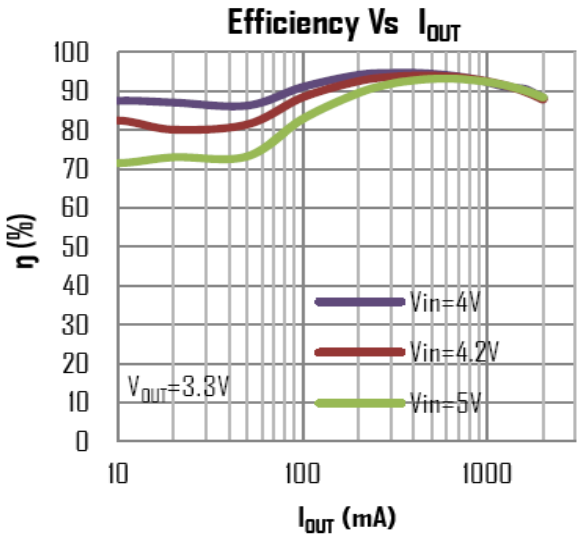
V_{IN}=V_{EN}=3.6V, and T_A=25°C unless otherwise specified.

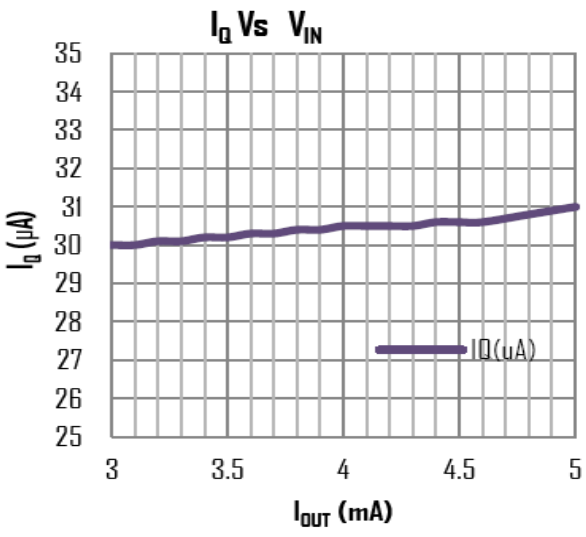
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	-	2.6	-	5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising	-	2.1	-	V
V_{UVHYS}	UVLO Hysteresis	V_{IN} falling	-	0.2	-	V
I_Q	Quiescent Current	V_{FB}=0.65V, I_{LOAD}=0mA	-	30	-	μA
I_{SHDN}	Shutdown Current	V_{EN}=0V	-	0.1	1.0	
V_{FB}	Feedback Voltage	V_{IN}=2.5V to 5.5V	0.588	0.600	0.612	V
V_{OUT}	Output Voltage Range	-	0.6	-	V_{IN}	V
$V_{EN(H)}$	EN Input High Voltage	-	-	-	1.5	V
$V_{EN(L)}$	EN Input Low Voltage	-	0.4	-	-	V
I_{EN}	EN Input Bias Current	-	-	-	1.0	μA
$R_{DS(ON)H}$	On Resistance of PMOS	I_{SW}=200mA	-	80	-	mΩ
$R_{DS(ON)L}$	ON Resistance of NMOS		-	100	-	
I_{LIM}	Peak Current Limit	-	-	2.5	-	A
I_{LKG}	SW Leakage Current	V_{EN}=0V	-	-	10	μA
REG_{LINE}	Line Regulation	V_{IN}=2.7V to 5.5V	-	0.04	-	%/V
REG_{LOAD}	Load Regulation	-	-	0.15	-	%/A
F_{OSC}	Switching Frequency	-	2.4	3.0	3.6	MHz
-	Thermal Shutdown Threshold	-	-	160	-	°C
-	Thermal Shutdown Hysteresis	-	-	15	-	°C

Typical Characteristics

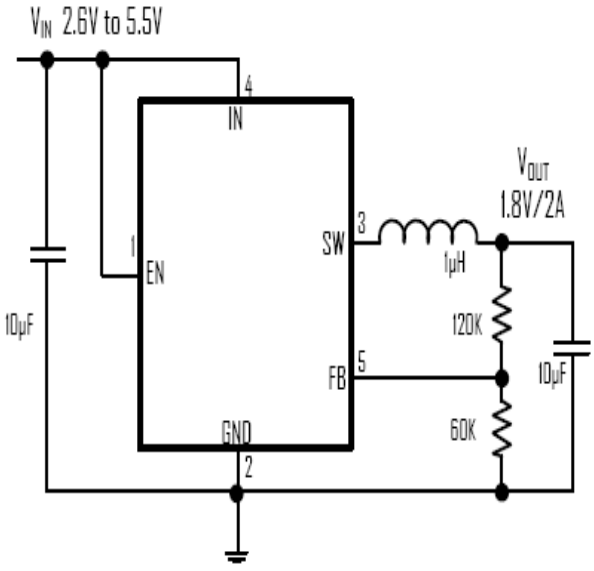


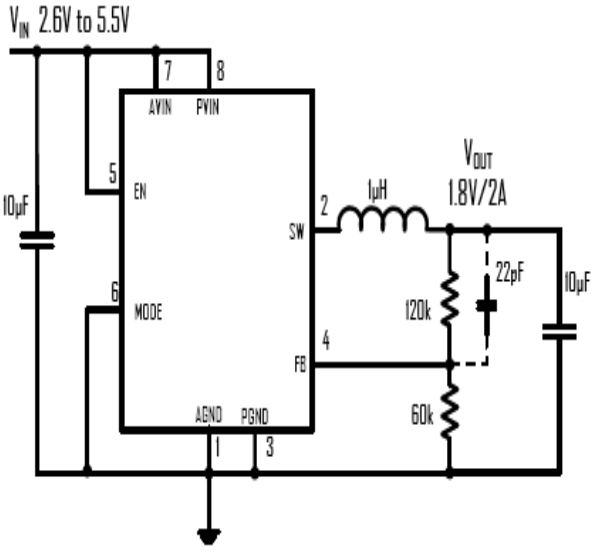






Typical Application Circuit





Functional Description

The GS5592 high efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 2A of output current. The device operates in pulse-width modulation (PWM) at 3MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to V_{IN}, making the GS5592 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Applications Information

Setting the Output Voltage

The internal reference V_{REF} is 0.6V(Typical).The output voltage is divided by a resistor,R1 and R2 to the FB pin. The output voltage is given by :

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2})$$

Loop Operation

GS5592 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. GS5592 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to I_{PEAK} and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

GS5592 has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below 1.9V, the UVLO circuit inhibits switching. Once IN rises above 2.1V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum over current trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. In this case, for 2A maximum output current, the maximum inductor ripple current is 667mA. The inductor size is estimated as following equation :

$$L=(V_{IN(MAX)}-V_{OUT}) / I_{RIPPLE}*D_{MIN}*(1/F_{OSC})$$

For V_{OUT}=1.8V.

The inductor values is calculated to be L = 1.0μH.

For V_{OUT}=1.2V.

The inductor values is calculated to be L = 0.47μH.

Applications Information (Continue)

Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability.

Output Capacitor Selection

For most applications a nominal 10μF or 22μF capacitor is suitable. The GS5592 internal compensation is designed for a fixed corner frequency that is equal to :

$$FC=\frac{1}{2*\pi\sqrt{COUT*L}} = 50Khz$$

For example, for V_{OUT}=1.8V, L=1.0μH, C_{OUT}=10μF, for V_{OUT} =1.2V, L=0.47μH, C_{OUT}=22μF

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows :

$$V_{RIPPLE} = I_{L(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, air flow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings air flow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

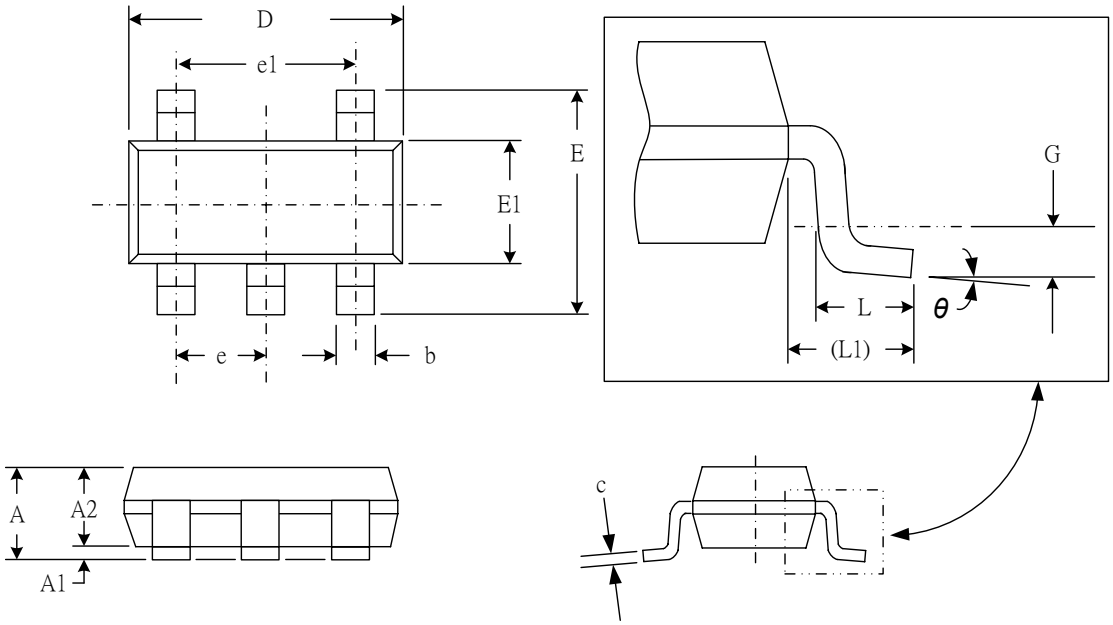
PCB Layout Recommendations

When laying out the printed circuit board, the following checking should be used to ensure proper operation of the GS5592. Check the following in your layout :

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Does the (+) plates of C_{IN} connect to V_{IN} as closely as possible. This capacitor provides the AC current to the internal power MOSFETS.
3. Keep the switching node, SW, away from the sensitive V_{OUT} node.
4. Keep the (-) plates of C_{IN} and C_{OUT} as close as possible.

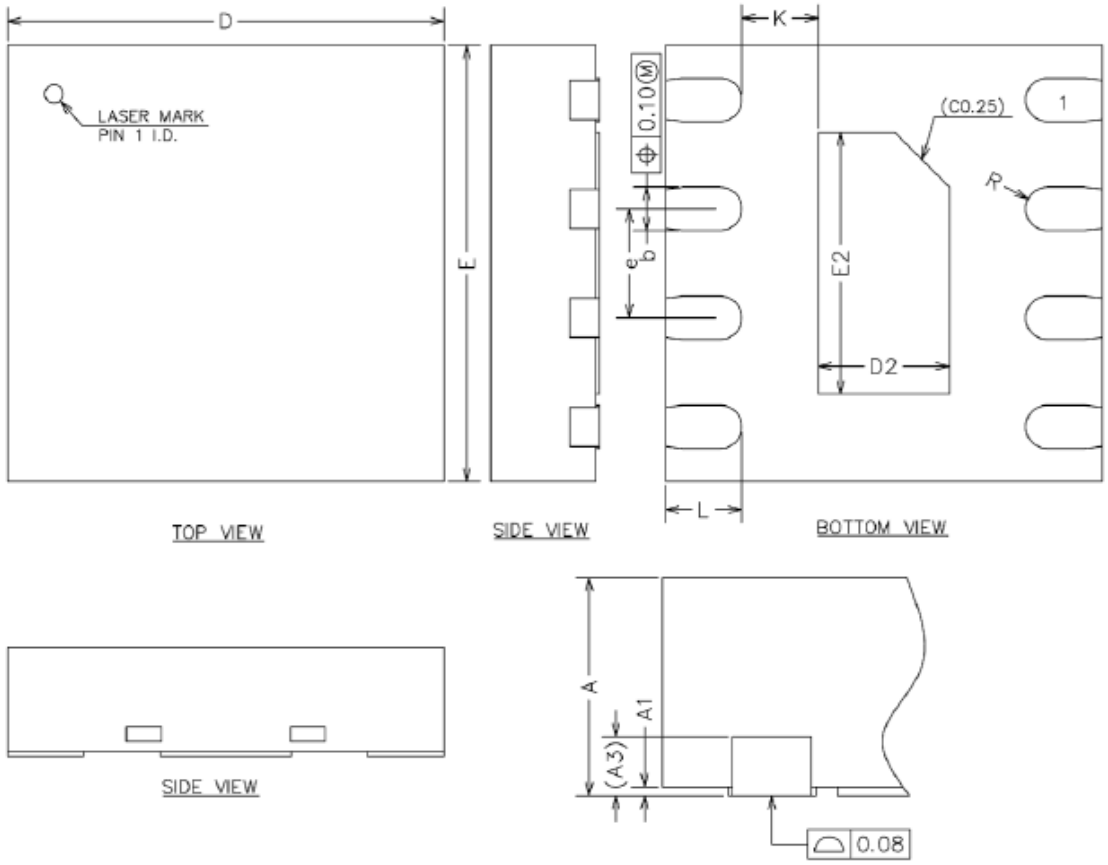
Package Dimension

SOT-23-5L PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.95	1.45	.037	.057
A1	0.05	0.15	.002	.006
A2	0.90	1.30	.035	.051
b	0.30	0.50	.012	.020
c	0.08	0.20	.003	.008
D	2.80	3.00	.110	.118
E	2.60	3.00	.102	.118
E1	1.50	1.70	.059	.067
e	0.95 (TYP)		.037 (TYP)	
e1	1.90 (TYP)		.075 (TYP)	
L	0.35	0.55	.014	.022
L1	0.60 (TYP)		.024 (TYP)	
G	0.25 (TYP)		.010 (TYP)	
θ	0°	8°	0°	8°

DFN2x2-8L PLASTIC PACKAGE



Dimensions

SYMBOL	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20(REF)			0.008(REF)		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.90	2.00	2.10	0.075	0.079	0.083
E	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.50	0.60	0.70	0.020	0.024	0.028
E2	1.10	1.20	1.30	0.043	0.047	0.051
e	0.40	0.50	0.60	0.016	0.020	0.024
K	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
R	0.09	-	-	0.004	-	-

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